HERMES

PAYLOAD DESIGN

Yuri Evangelista
INAF-IAPS

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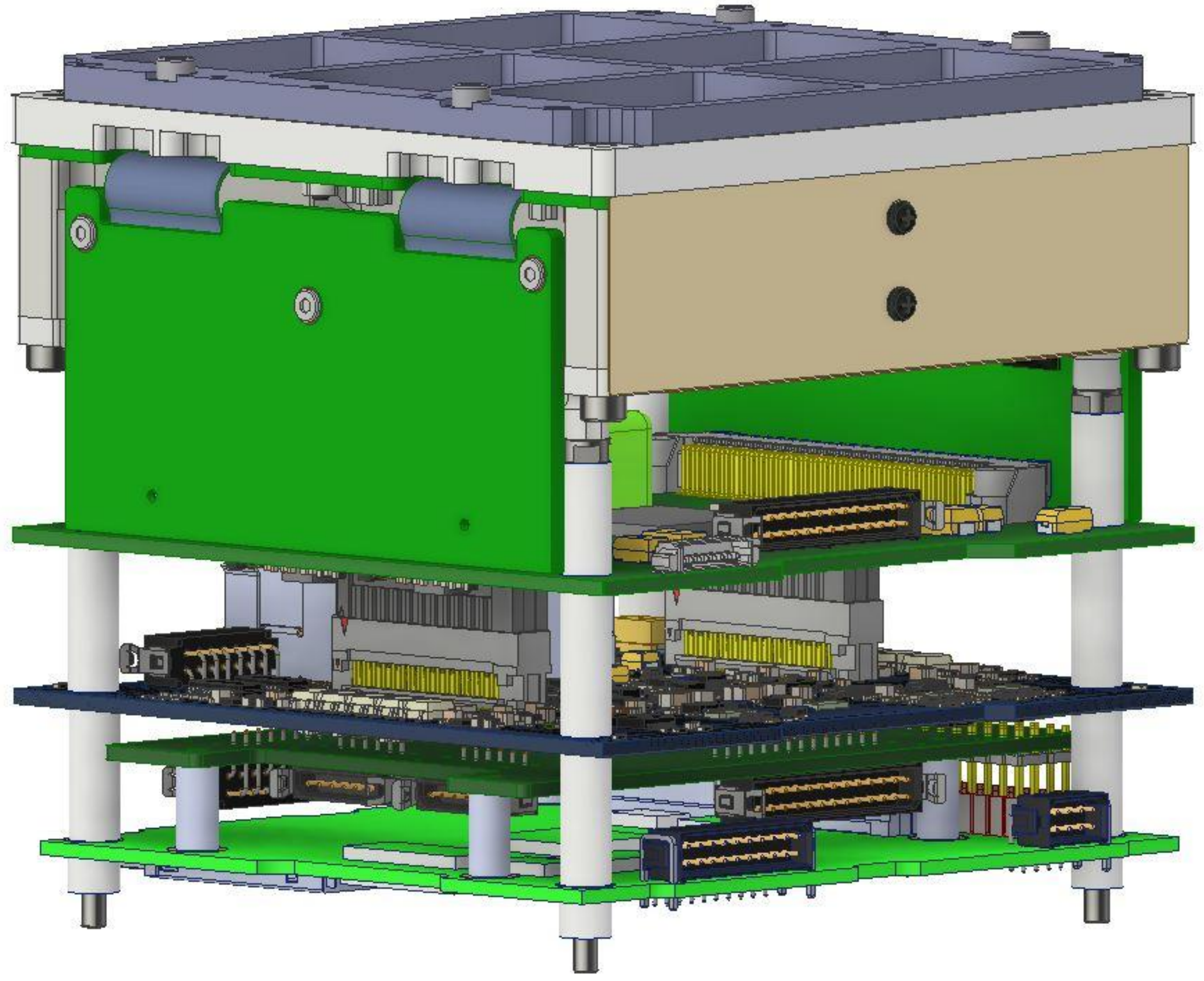
The HERMES team acknowledges financial support from the Accordo Attuativo ASI-INAF HERMES Technological Pathfinder No 2018-10-H.1-2020

HERMES P/L REQUIREMENTS

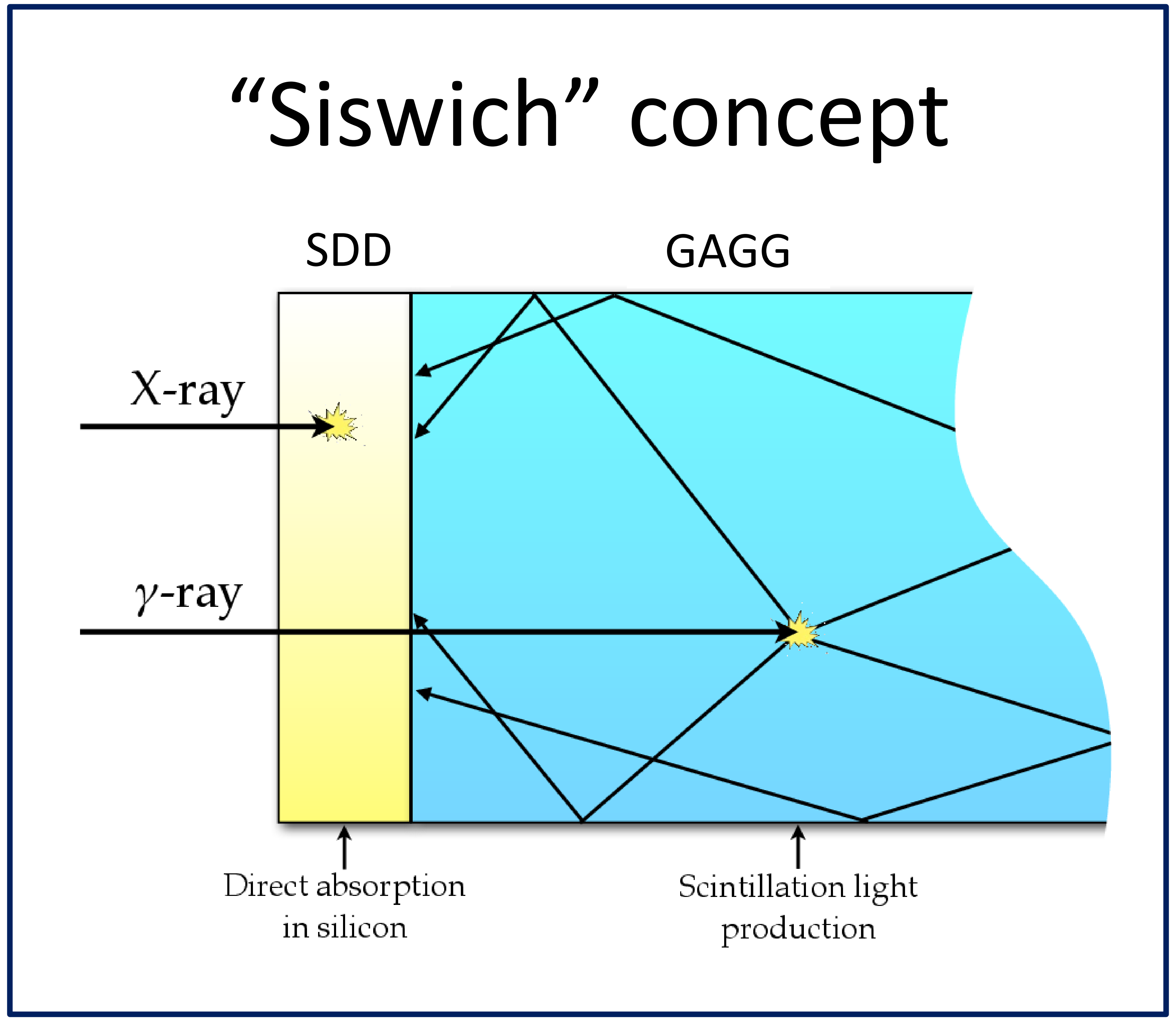
- **SENSITIVITY** → better than 2 ph/cm^2/s
- **EFFECTIVE AREA** → larger than 50 cm^2
- **ENERGY BAND** → E_{low} ≤ 5 & E_{high} keV ≥ 2 MeV
- **ENERGY RESOLUTION** → better than 1 keV (X) and 5 keV (γ) EOL
- **TIME RESOLUTION** → better than 400 ns
- **TIME ACCURACY** → better than 200 ns
- **FOV** → larger than 3 sr FHWM
- **BACKGROUND** → lower than 12 counts/cm^2/s

- **VOLUME** → smaller than 1.25 U
- **MASS** → lower than 1.8 kg
- **POWER** → lower than 5 W
- **RADIATIVE ENV** → LEO (EQ or SSO)
- **THERMAL CONTROL** → passive
- **COMPONENTS** → COTS (mainly)
- **RELIABILITY** → higher than standard CubeSats
- **REDUNDANCY** → segmented detector
- **OTHER** → “mass” production



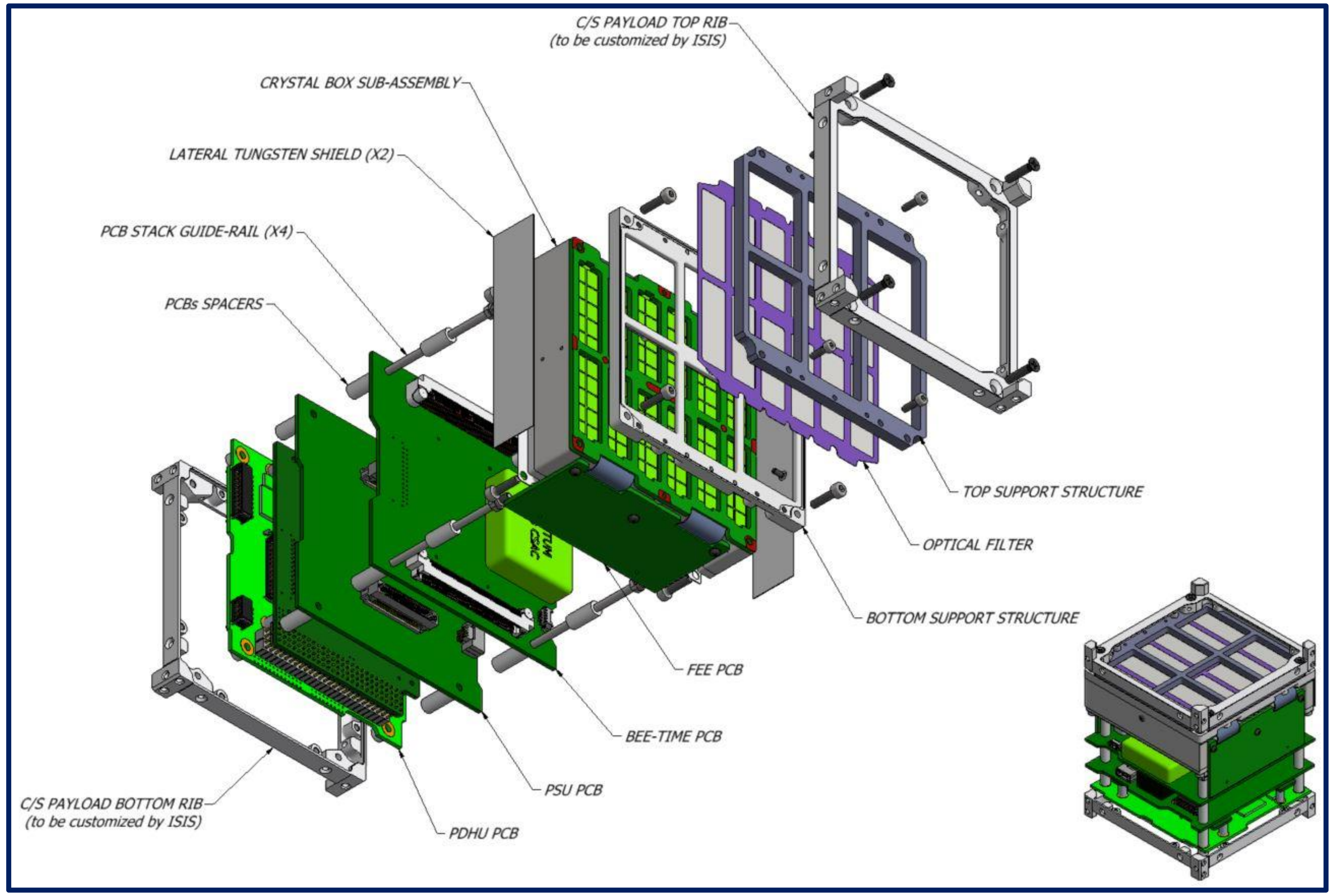
DETECTOR WORKING PRINCIPLE

Compact and lightweight instrument with a very wide sensitivity band



- Silicon drift detectors (SDD) as direct X-ray and "indirect" gamma-ray (scintillator light) detectors
- GAGG scintillator crystals
- Custom designed front-end and back-end ASICs
- Custom designed BEE and PSU electronics
- Very compact (96x96x30 mm^3)

P/L SUBSYSTEMS



Detector assembly – INAF, INFN, PoliMi, UniPV, FBK, IHEP

- Detector Support Structure (provides mechanical I/F, FEE stiffness, hosts the optical filter)
- Front-End Electronics (FEE) (hosts: 12 Silicon Drift Detector (SDD) arrays, each with 10 independent cells; 120 LYRA-FE ASIC dies; 4 LYRA-BE ASICs; 2 connectors toward the BEE; 6 temperature sensors)
- 60 GAGG scintillator crystals (optically isolated on 5 sides), optically connected to the SDD through a space qualified silicone pad)
- Crystal box (with 200 µm Tungsten shields

Back-End Electronics (BEE) – INAF

- FEE electrical I/F
- A/D conversion
- Time generation and time tagging (baseline solution)
- Data preformatting

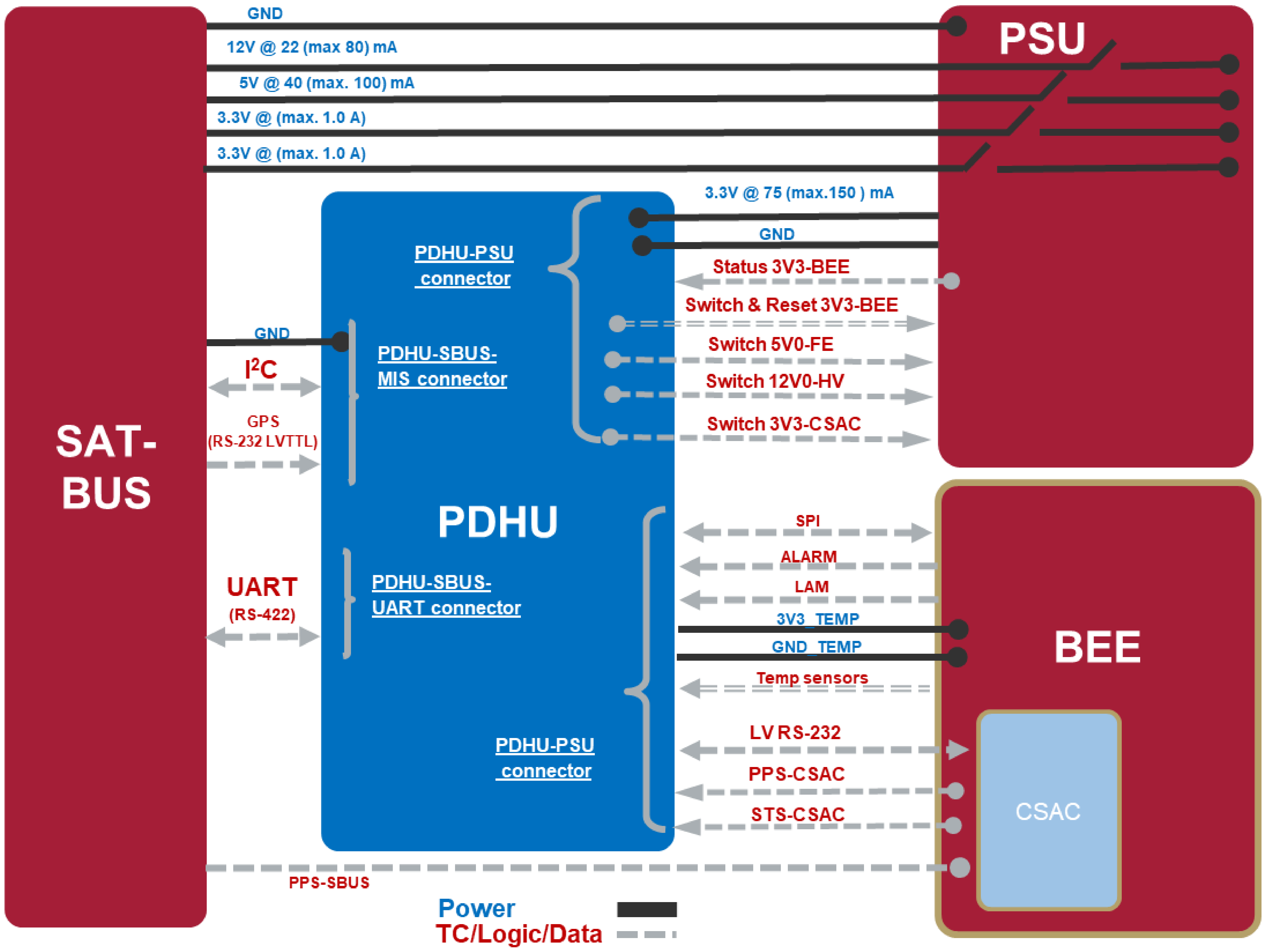
Power Supply Unit (PSU) – INAF

- I/F to S/C power bus
- Generation, control and monitoring of P/L power supplies;
- Latch-up control

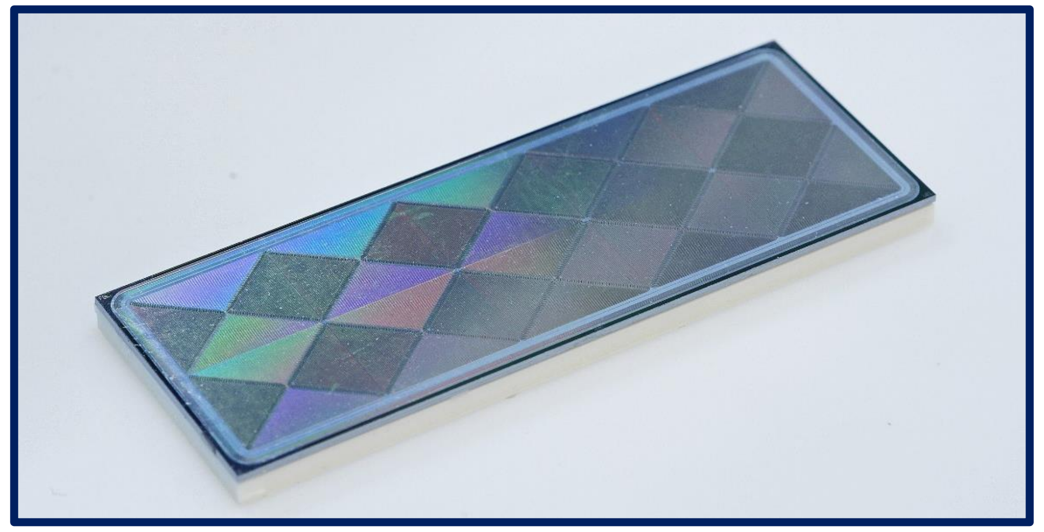
Payload Data Handling Unit (PDHU) – University of Tubingen

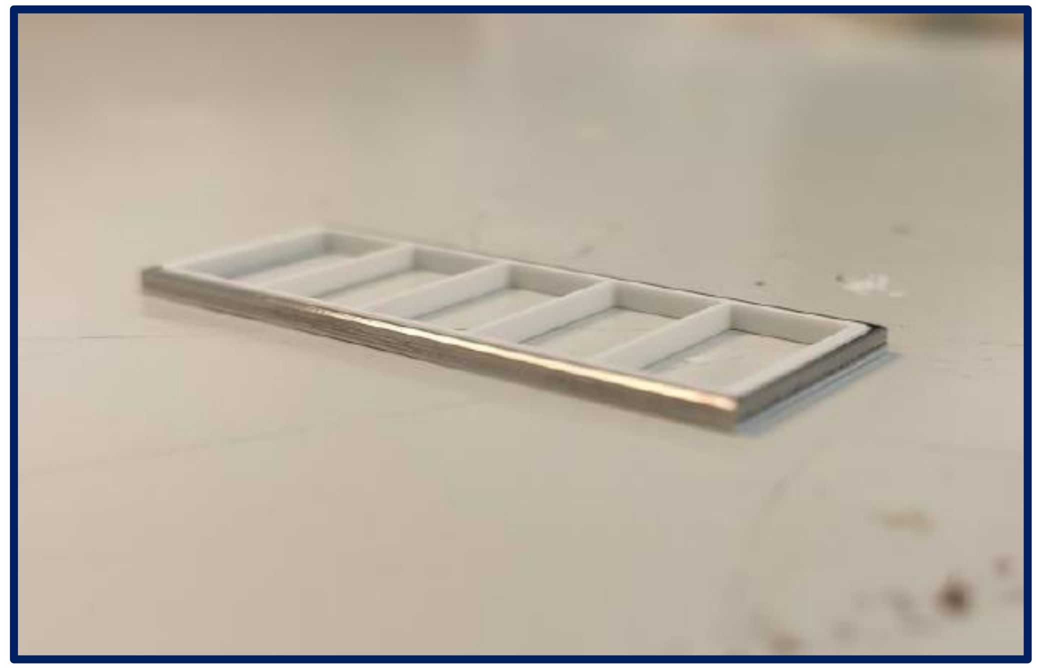
- onboard computer
- manage FEE and BEE configuration
- Data formatting
- Burst search
- TM/TC interface

P/L ELECTRICAL INTERFACES



SILICON DRIFT DETECTORS



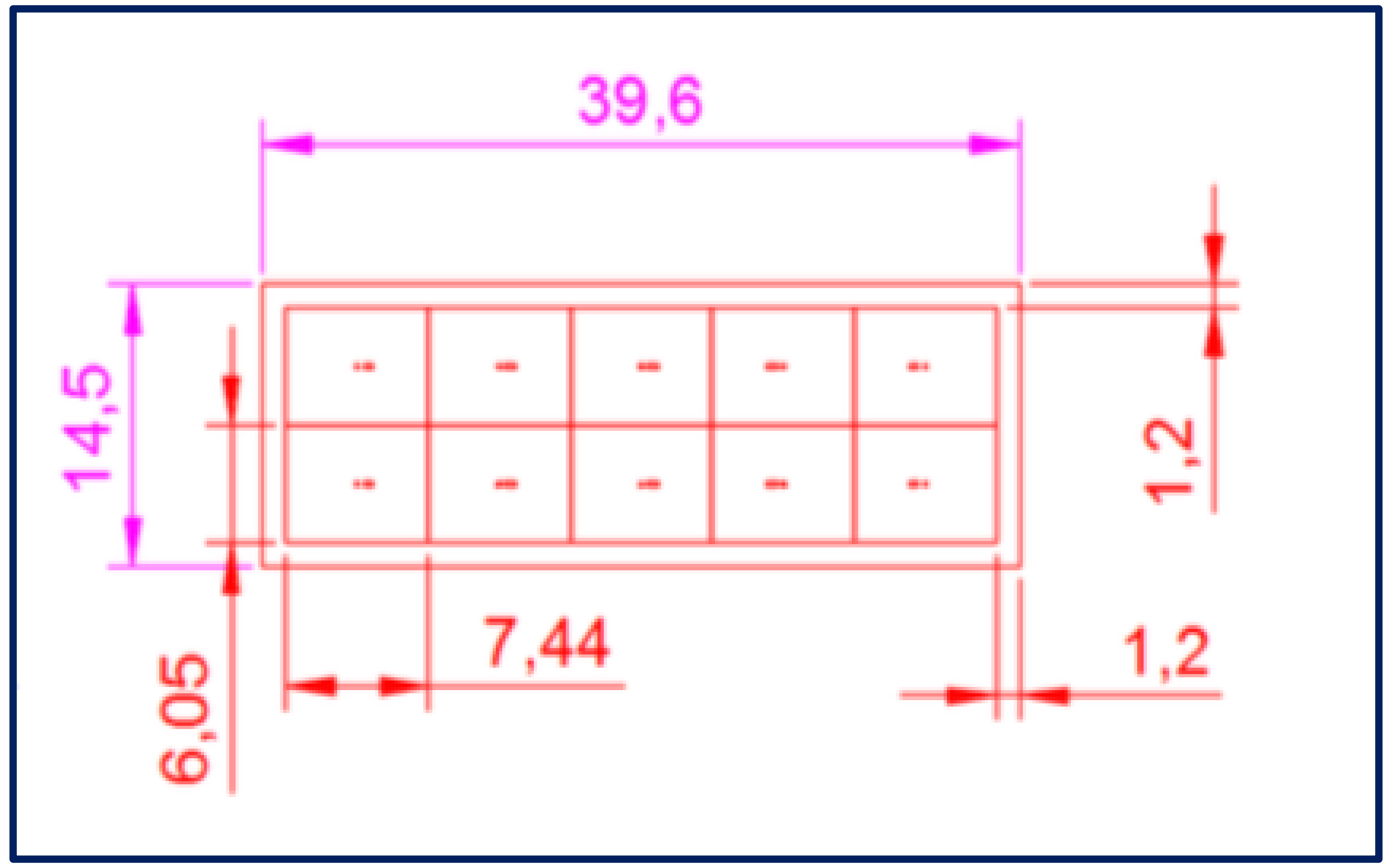


State-of-the-art results achieved within the framework of the Italian ReDSoX collaboration. Strong synergy between INFN-Trieste and Fondazione Bruno Kessler (FBK, Trento) for design/production, funding by ASI, INAF and INFN for design consolidation and space qualification (LOFT & HERMES)

Baseline detectors for eXTP (LAD, WFM) and THESEUS (XGIS)

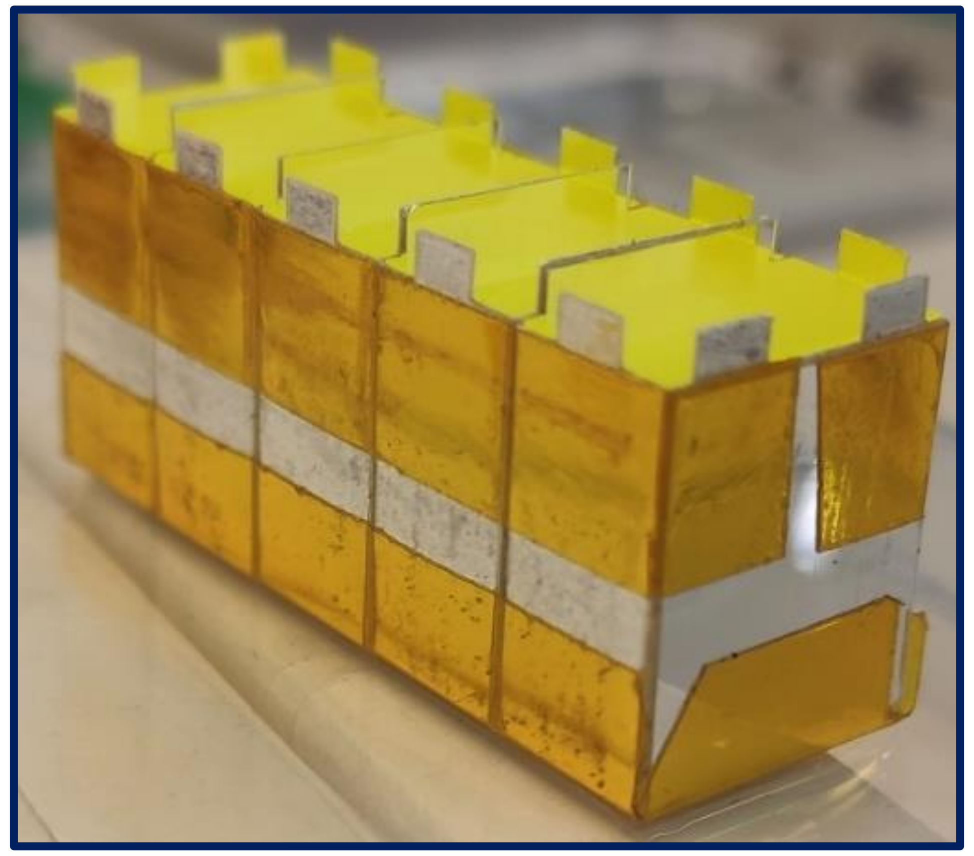
Design optimized for:

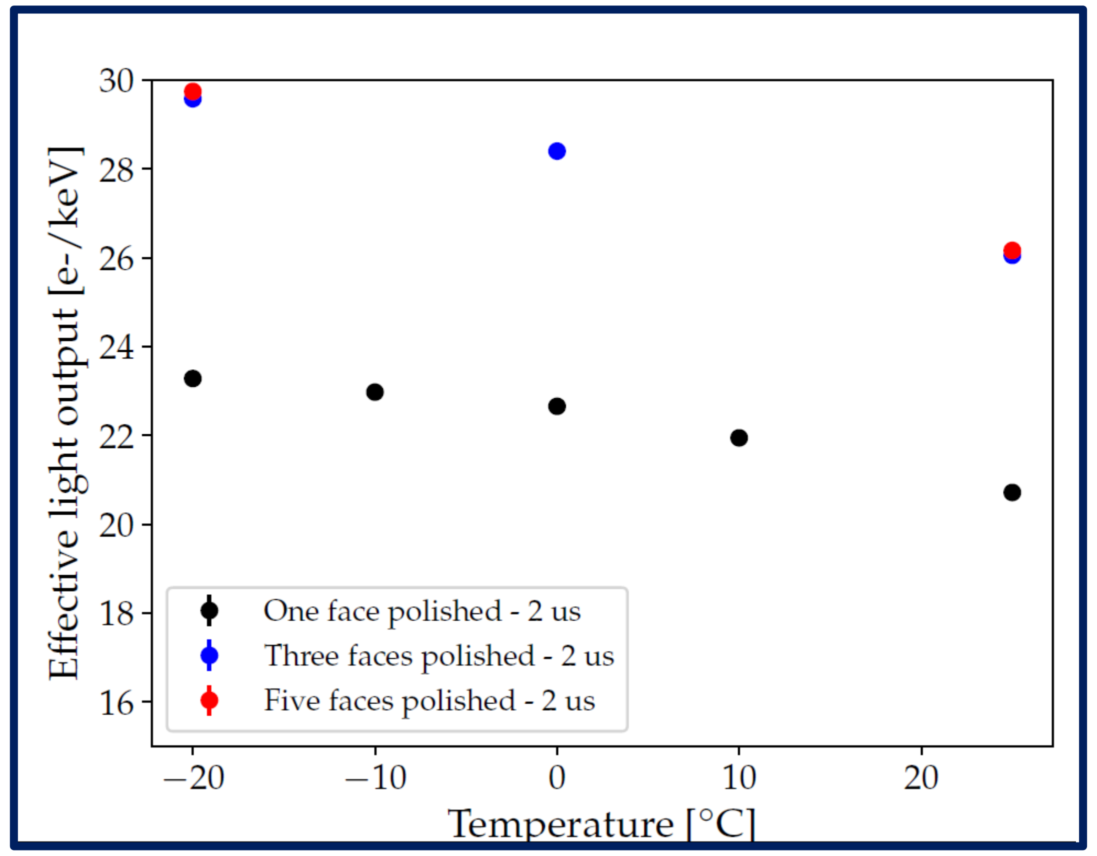
- Energy resolution and noise (threshold)
- Modularity (redundancy)
- FEE PCB complexity and integration
- Time resolution
- X/gamma discrimination (via multiplicity)
- Resources (i.e. power consumption, bias voltages)



GAGG SCINTILLATORS

	LaBr3(Ce)	NaI(Tl)	CsI(Tl)	GAGG	GFAG	BGO
Density [g/cm3]	5,08	3,67	4,51	6,63	6,7	7,13
Lambda max [nm]	380	415	560	520	520	480
Decay time [ns]	16	250	1000	88	45	300
Hygroscopic?	yes	yes	no	no	no	no
Light yield [ph/keV]	63	38	54	57	45	8
Energy res @662 keV [%]	2,6	7	5	5,2	5	10
Rise time				200 ps		
Radioactive?	yes	no	no	no	no	no



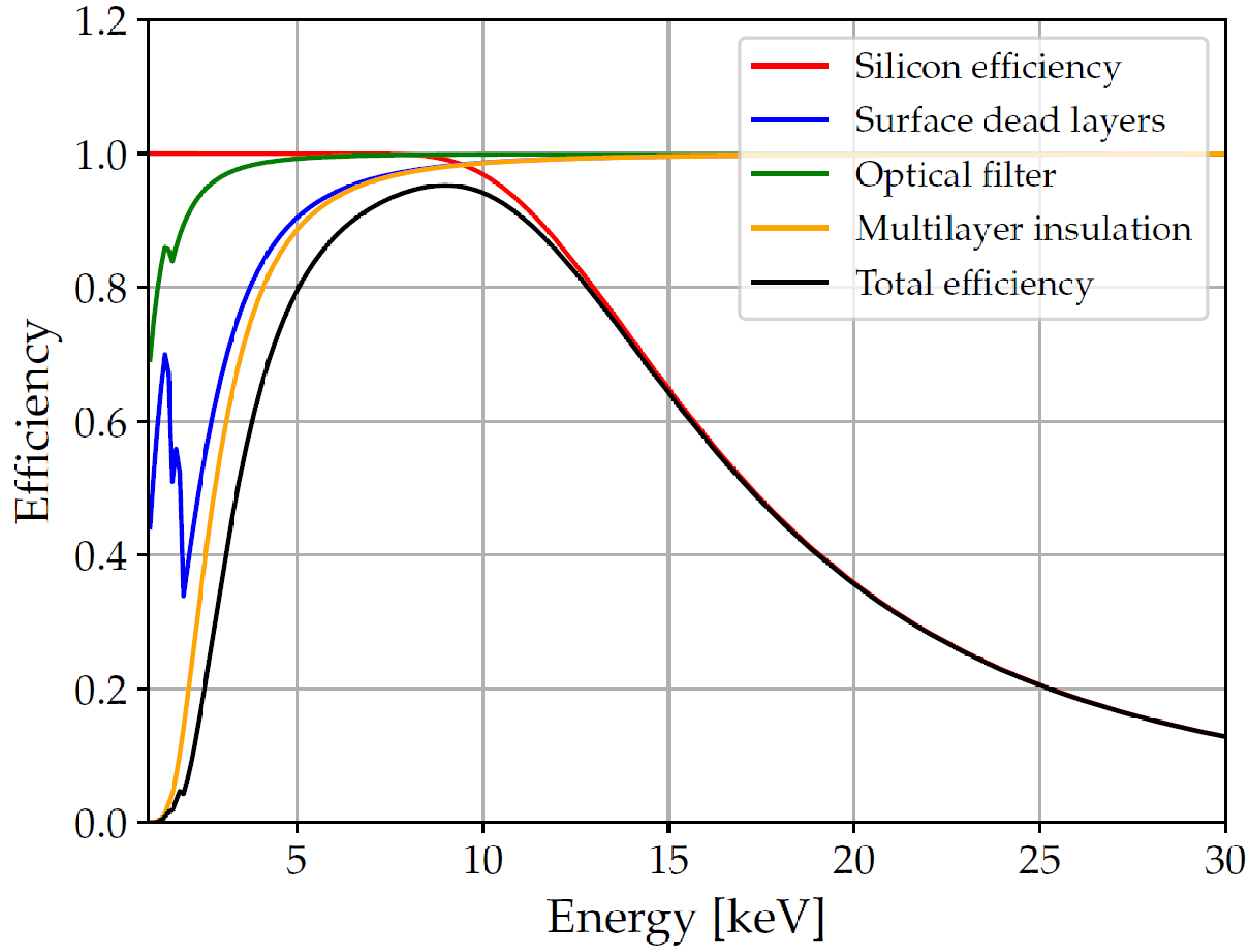


GAGG crystals:

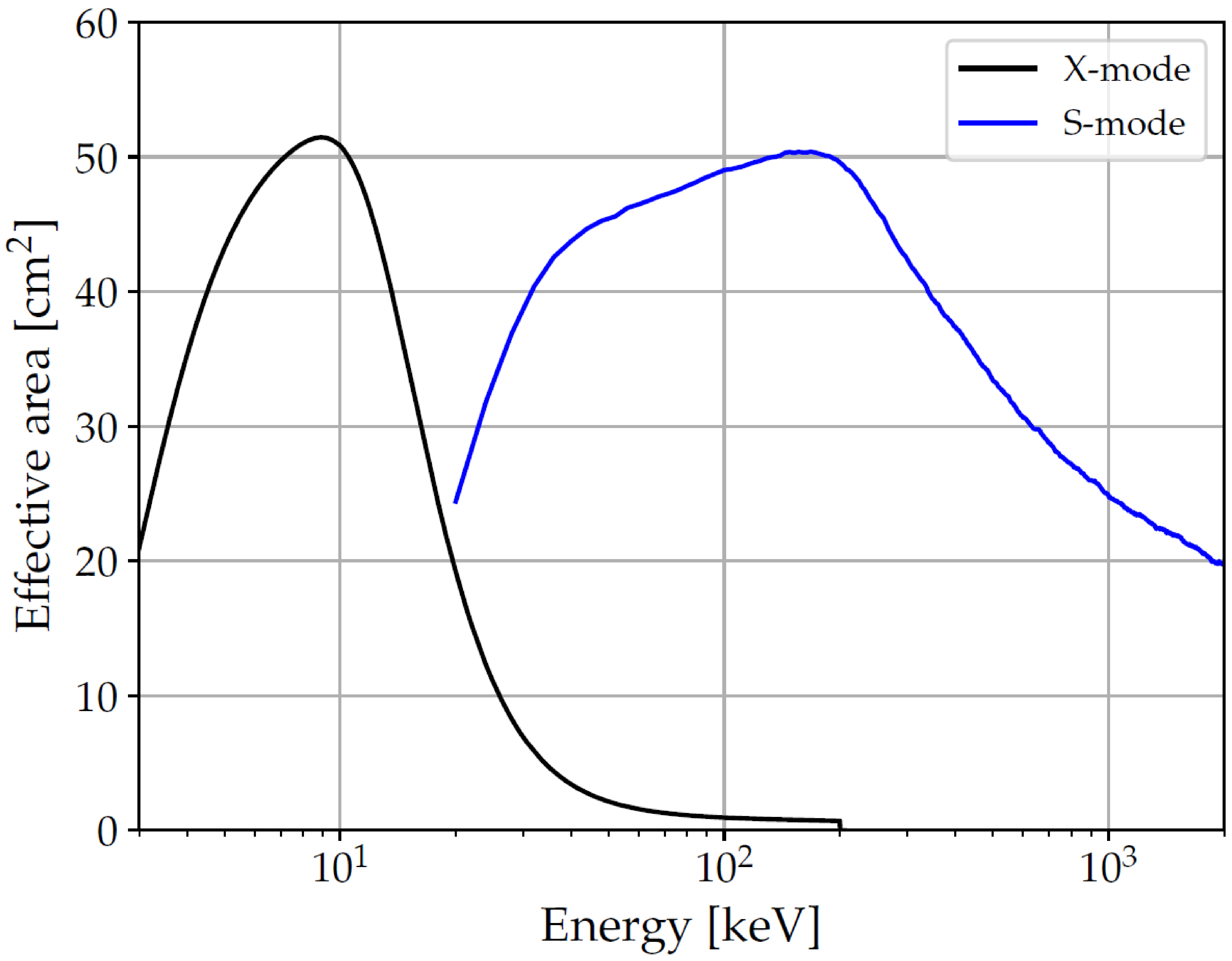
- High stopping power, fast response, optimal lambda max for Si coupling
- Not hygroscopic
- Not radioactive
- Radiation tolerant (athough not flight proven so far due to SiPM failure - GRID)
- Proton irradiation in the framework of the HERMES project
- Geometrical design, surface finishing and wrapping procedure optimized for light output (i.e. energy resolution and lower E_{thr})

EFFECTIVE AREA BREAKDOWN

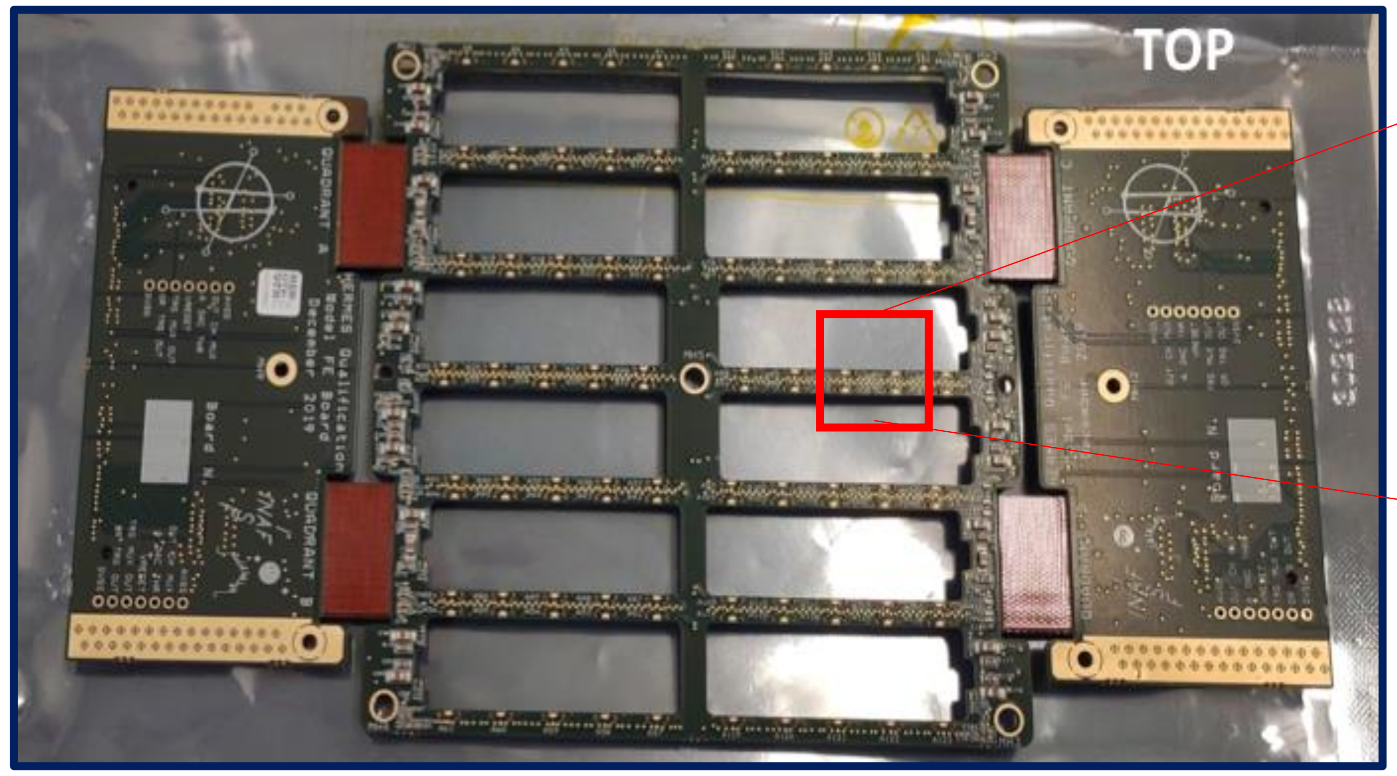
SDD Efficiency

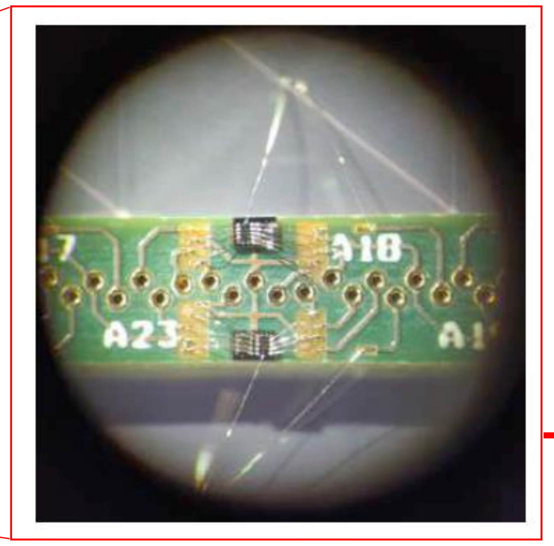


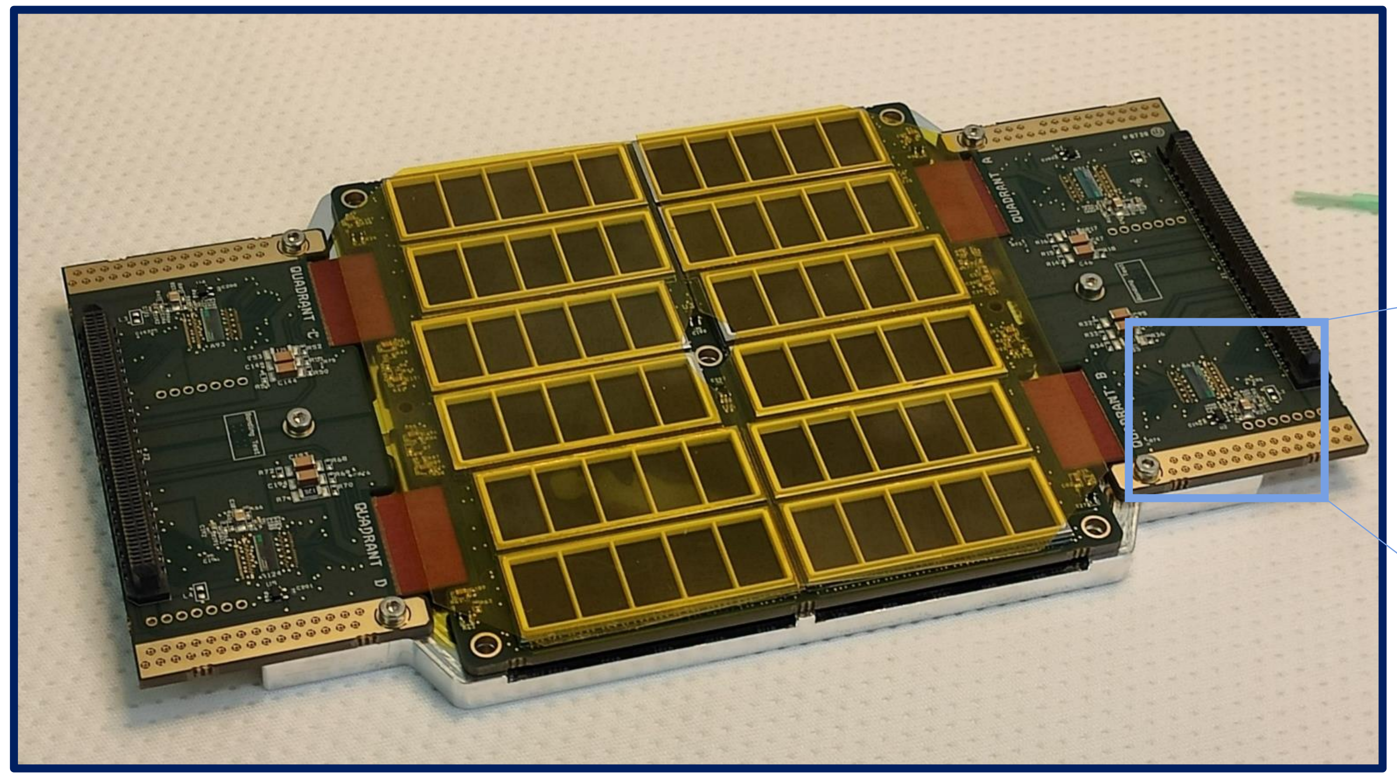
Effective Area

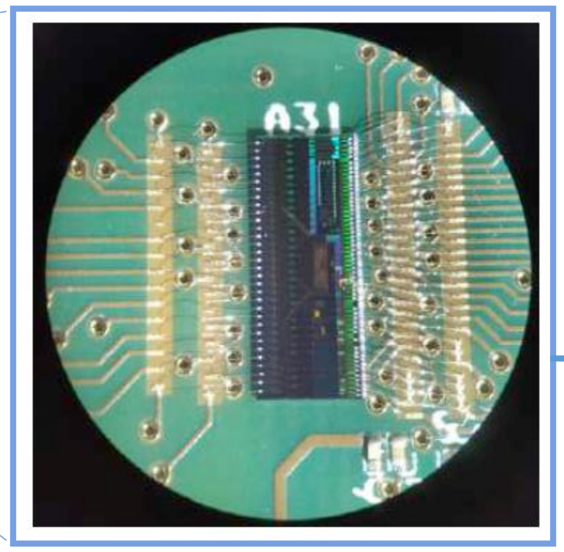


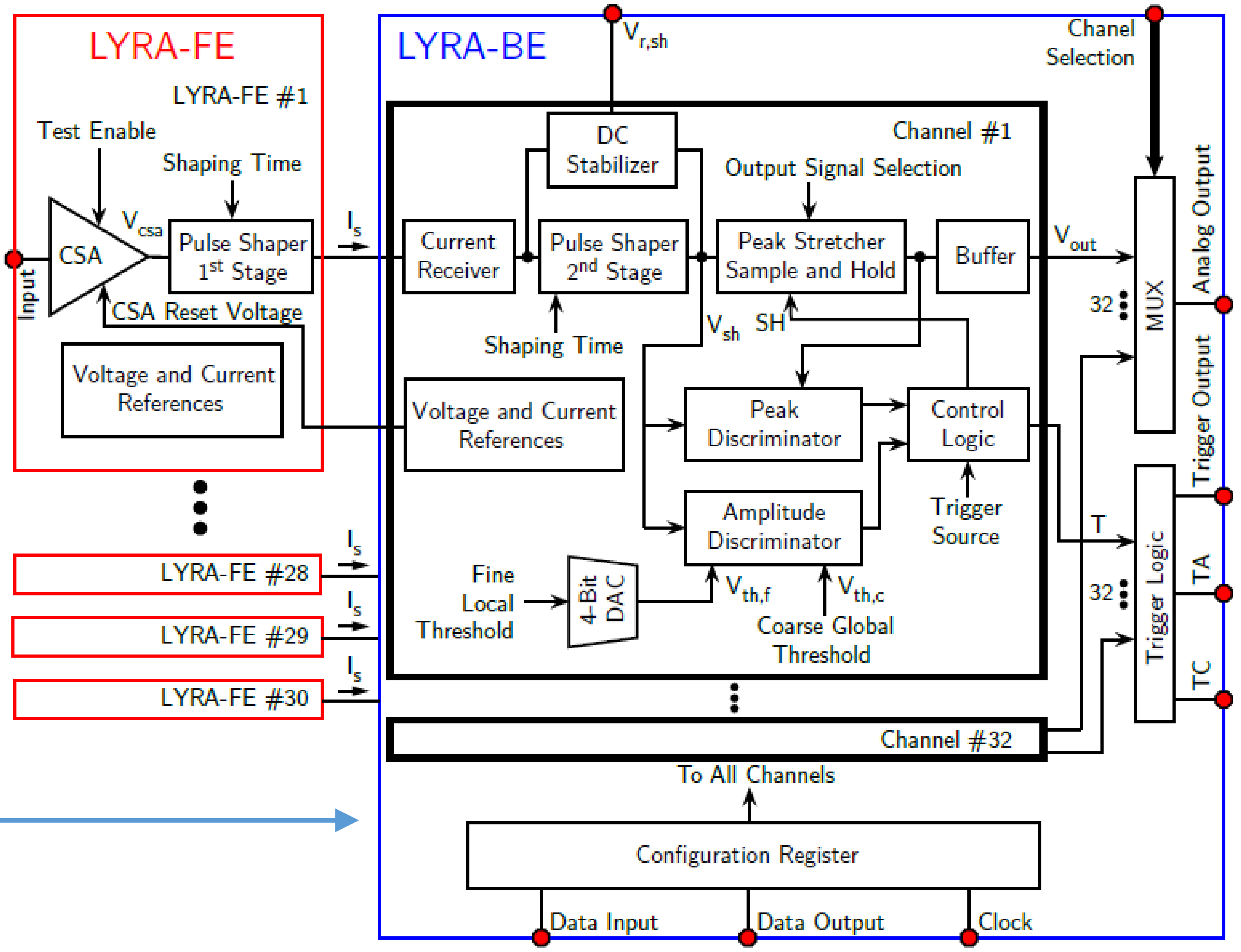
FEE PCB & READOUT ASIC









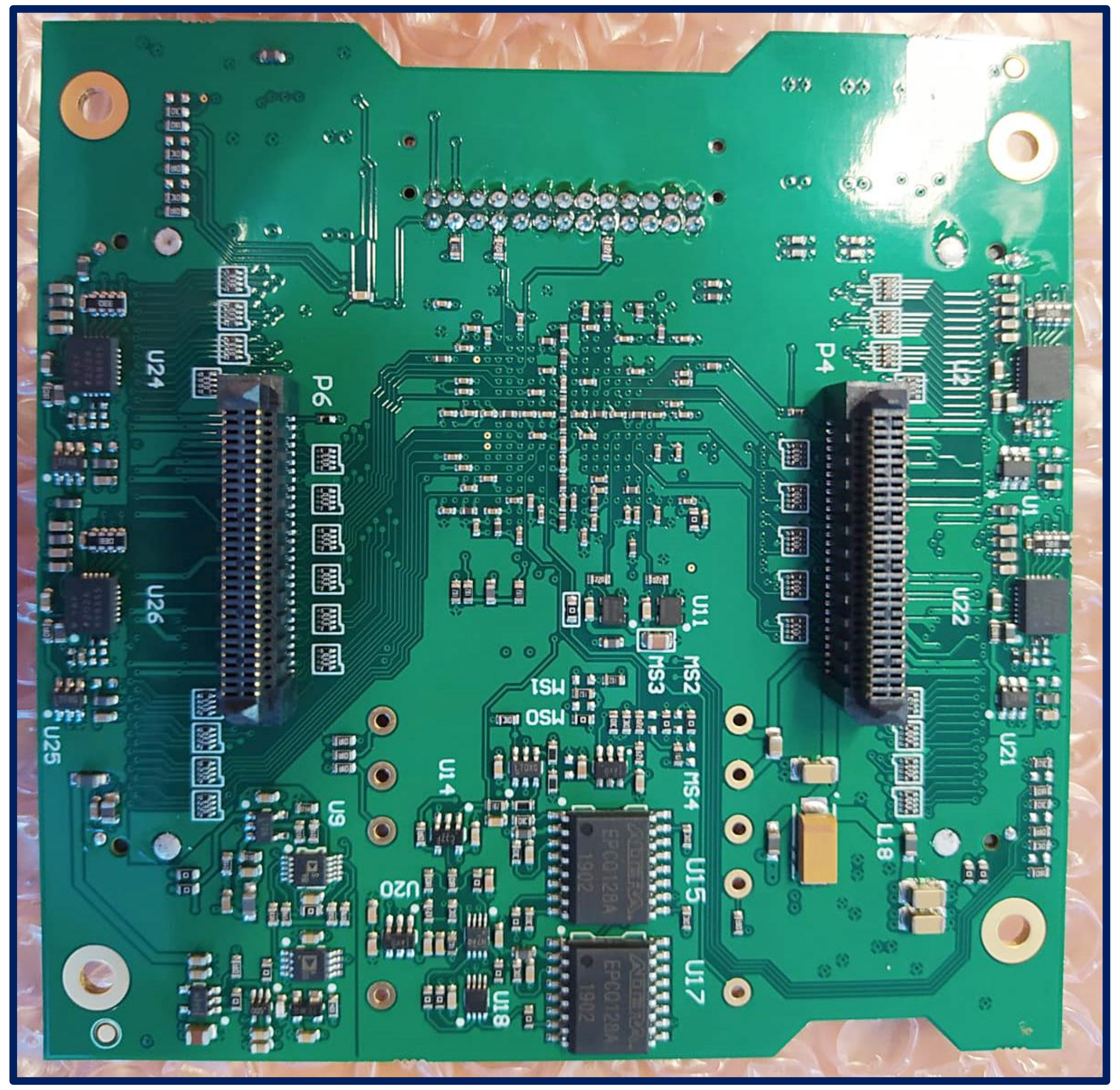


State of the art ASICs developed by PoliMi and UniPavia (with long heritage on SDD readout)

ASIC and FEE design optimized for:

- Noise performance (also leakage & capacitance matching)
- Energy range: 0-33000 e^- (0÷120 keV in Si, 0÷2.5 MeV in GAGG)
- Low power: < 1mW/channel
- Signal routing and low cross-talk (I-based I/F, separation in LYRA-FE and LYRA-BE)
- Rad. tol. technology (AMS 0.35) with flight heritage (e.g. Solar Orbiter)

BEE & PSU BOARDS



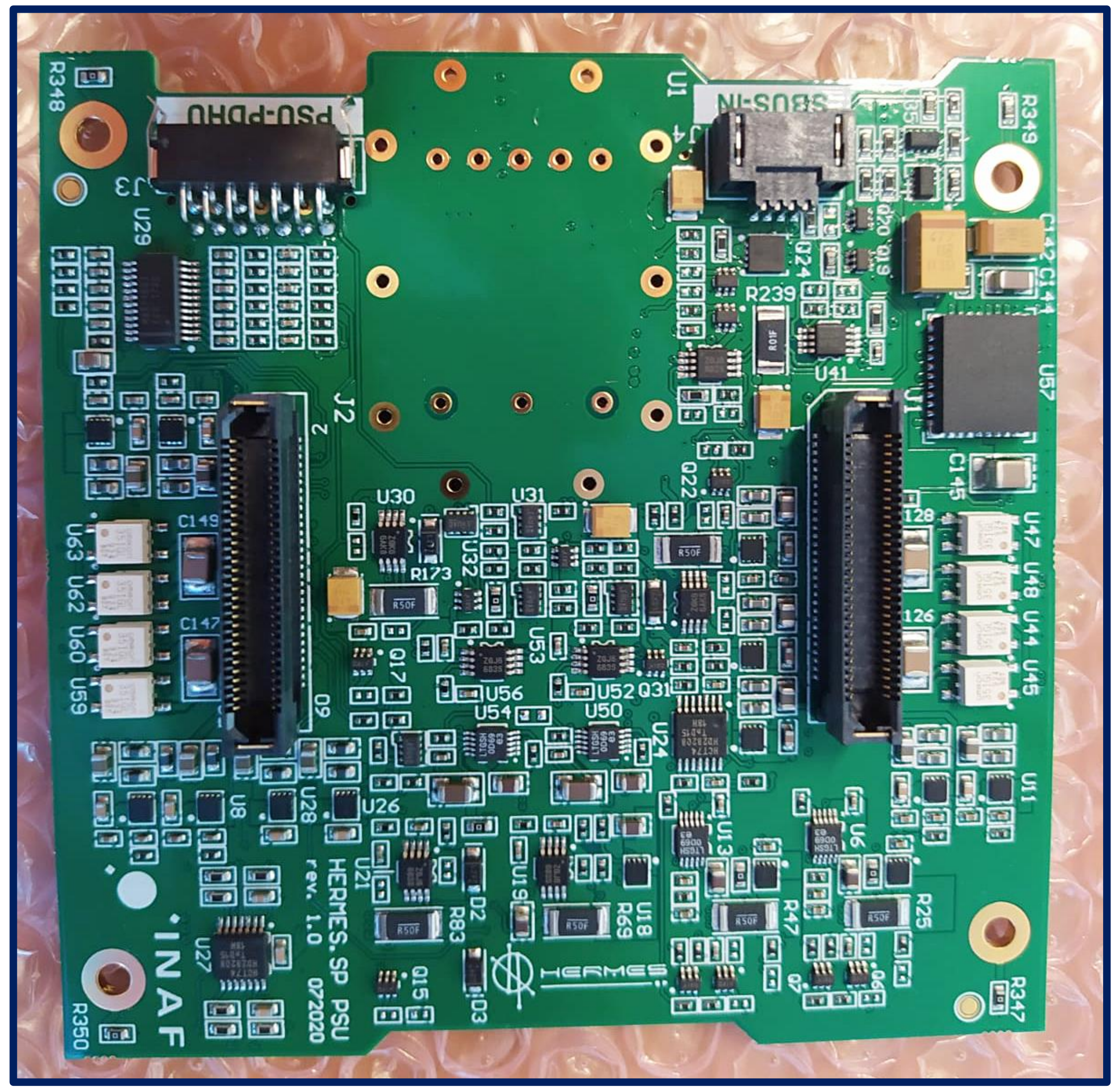
BEE tasks/functionalities

The core of the BEE is a SEL immune Intel/Altera Cyclone V FPGA

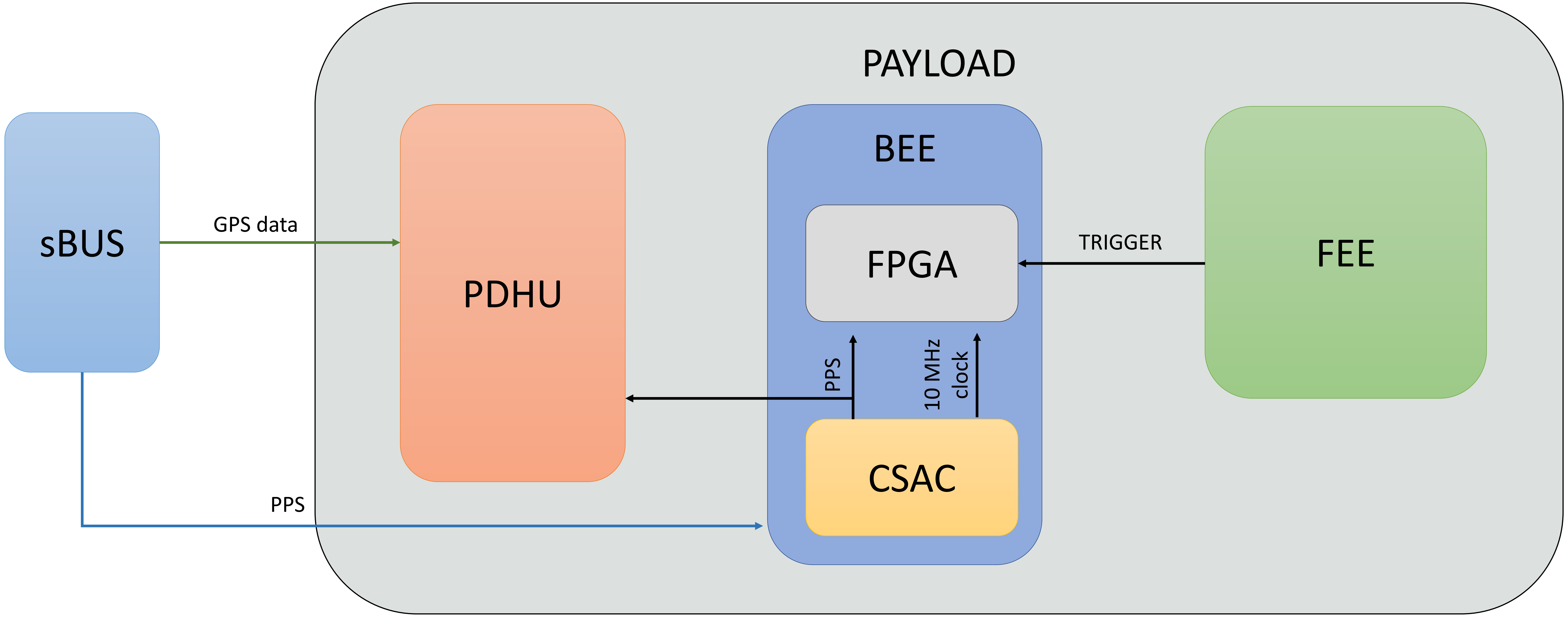
- ASICs Configuration
- Logic for Event Trigger Detection and Acquisition
- Generation of a configurable test pulse for in-flight calibration
- HKs collection
- TCs parser
- Time-tagging management (local rad-hard Chip Scale Atomic Clock – CSAC)

PSU tasks/functionalities

- SDD High Voltage (-120V) generation and ramp-up/ramp-down
- Overcurrent protection for 12V rail (primary of HV DC-DC)
- Overcurrent/latch-up protection for BEE PS
- Overcurrent/latch-up protection for LV rails (FEE)
- Ultra low-noise, high PSRR LDOs for FEE LV
- Independent low voltage and high voltage load switches for each quadrant
- Controlled detector switch-off in case of latch-up/anomaly



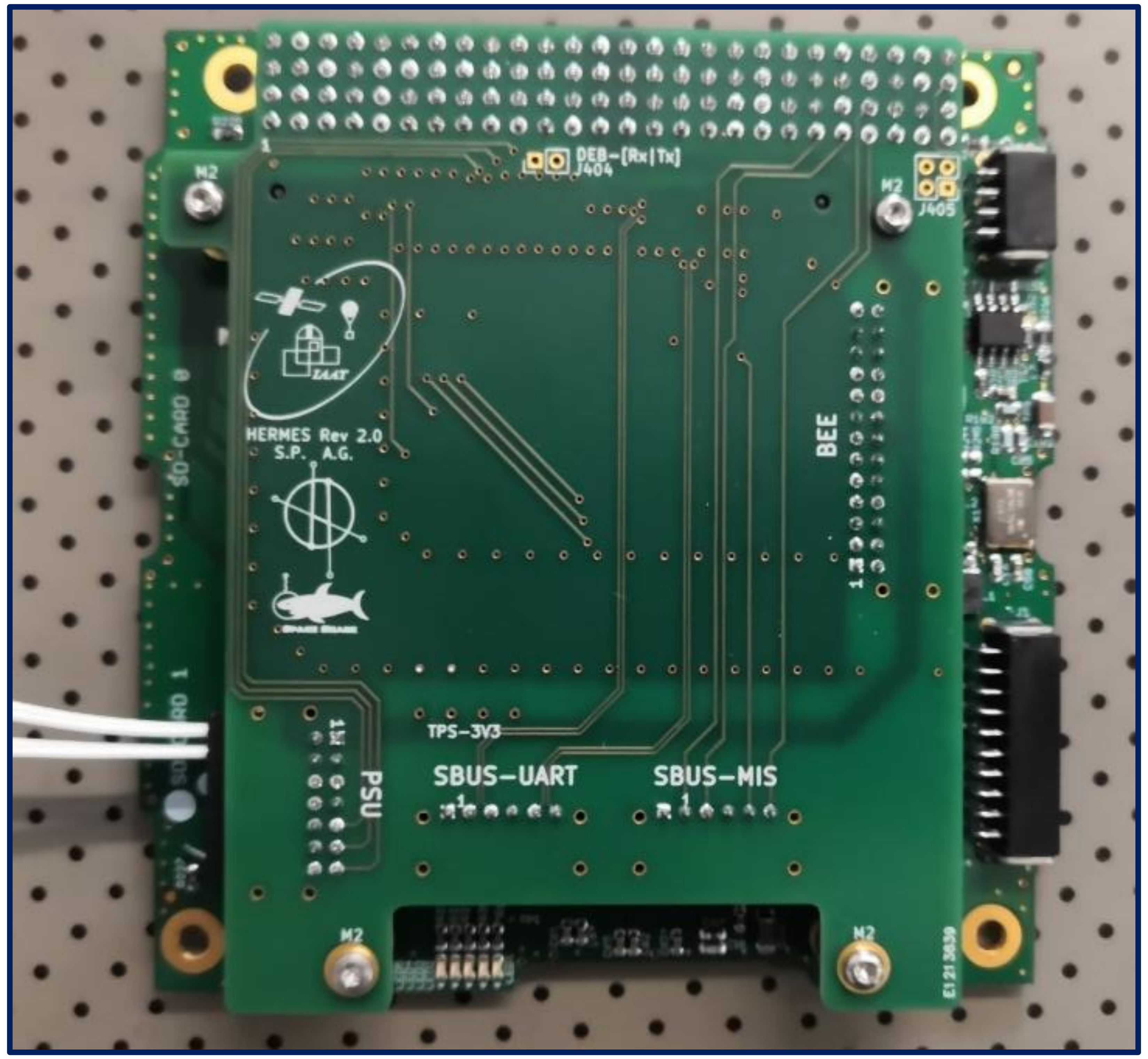
TIMING ARCHITECTURE



Overall time measurement precision (GPS/PPS locked)			
Mode	**Time accuracy (68% c. l.)**	**Time resolution (68% c. l.)**	**Total (68% c. l.)**
X-Mode	53.4 ns	320 ns	324 ns
S-mode	53.4 ns	216 ns	222 ns

Overall time measurement precision (GPS/PPS unlocked)			
Mode	**Time accuracy (68% c. l.)**	**Time resolution (68% c. l.)**	**Total (68% c. l.)**
X-Mode	181 ns	320 ns	368 ns
S-mode	181 ns	216 ns	282 ns

PDHU

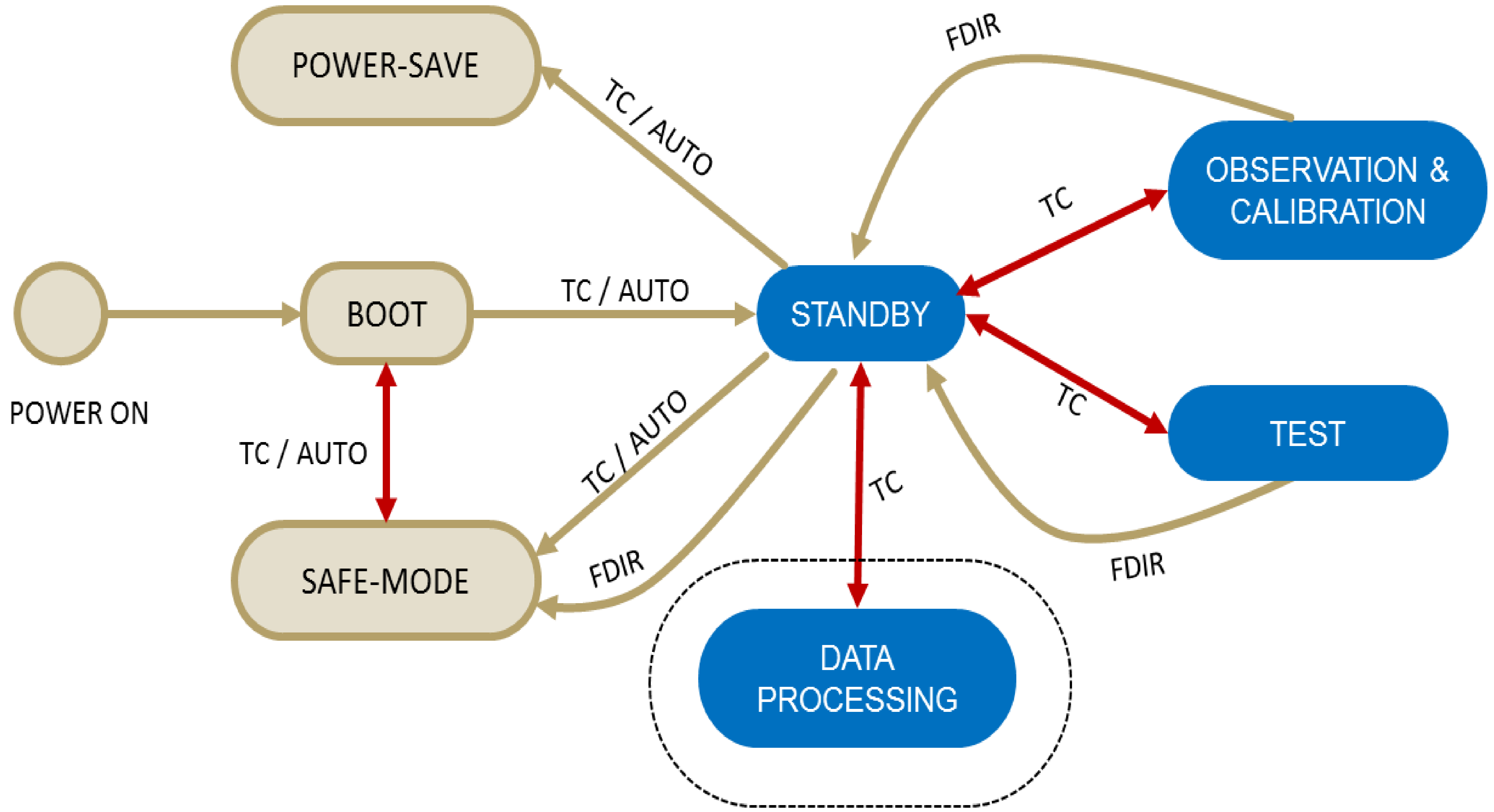


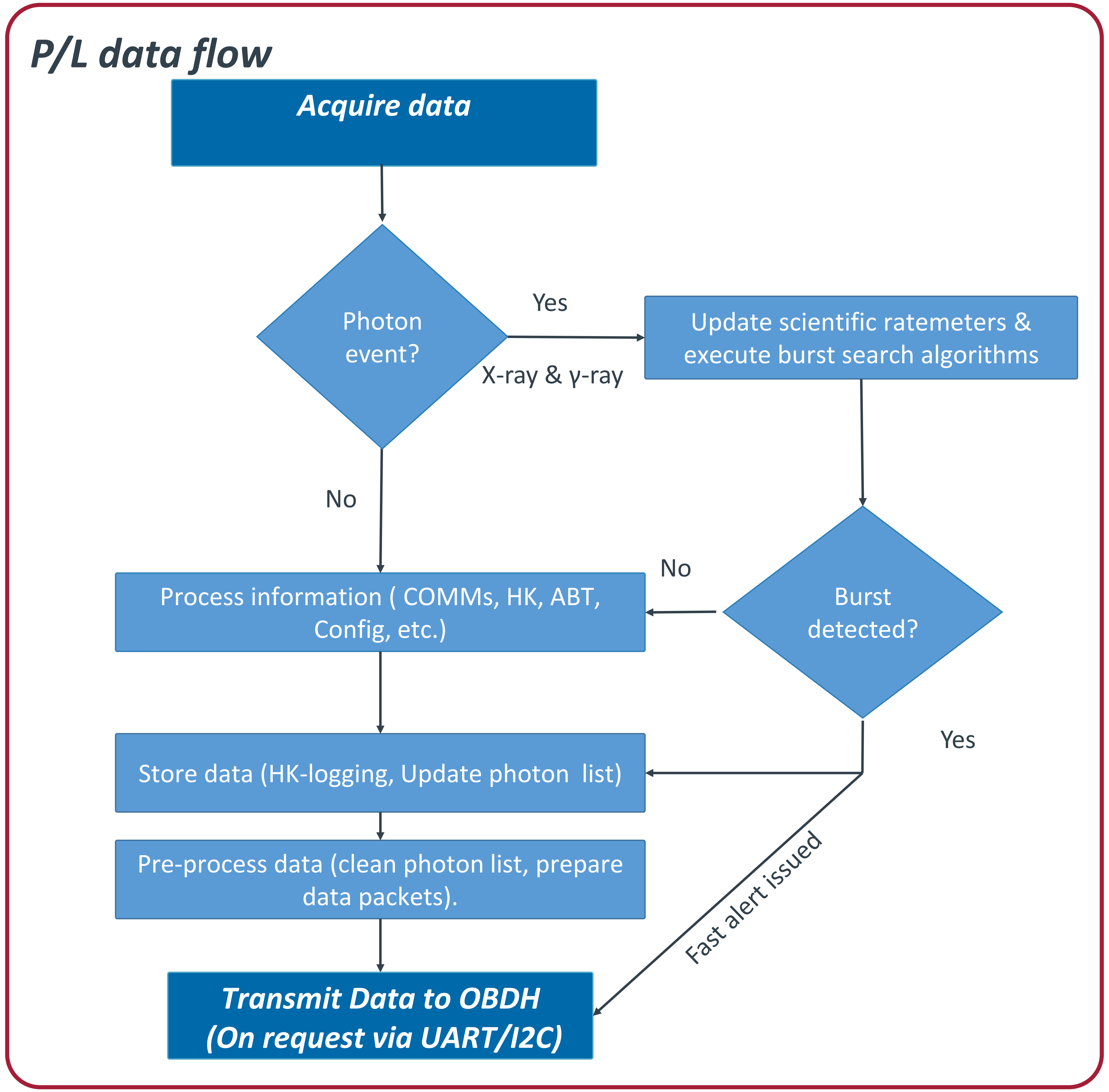
- Based on the ISIS On-Board computer (iOBC).
- Flight proven ARM9 processor.
- Power efficient (~380 mW)
- On-board: telemetry, voltage, current and temperature sensors
- External on-board watchdog and power-controller
- High reliability data storage (SD Cards) with FailSafe file system
- Volatile memory 64 MB SDRAM, Code storage 1 MB NOR Flash
- Critical data storage 256 kB FRAM
- Flexible daughterboard architecture
- SW development and deep customization by University of Tubingen

PDHU tasks:

- P/L interface with sBUS
- Operative mode management
- Photon list generation & events buffering
- Photon list 'cleaning' (e.g. particles filt.)
- Burst trigger logic management
- Scientific Data packet formatting
- Housekeeping (HK) management
- CSAC I/F
- Mass memory

P/L OPERATIVE MODES & TELEMETRY MANAGEMENT





SCIENTIFIC TELEMETRY

PDHU SRs				
	Sampling [s]	Packet size [byte]	Packet size [bit]	Rate [bit/s]
PDHU SR (4 quadrants, 3 energy bands, 7 timescales)	60	840	6720	112

Scientific ratemeters (4 quadrants, 3 energy bands, 7 timescales) produced & stored on the fly. Rready for prompt IRIDIUM transmission in case of trigger

PHOTON LIST				
	Sampling [s]	Packet size [byte]	Packet size [bit]	Rate [bit/s]
UTC reference	1*	9	72	72
BEE Analog and digital HKs	1	64	512	512
Detector temperatures	1	24	192	192
Number of entries	1*	4	32	32
ABT event	1	8	64	64
			SUBTOTAL	872
Photon events	N/A	8	64	N/A

BACKGROUND PHOTON-BY-PHOTON					
Component	evt/s	bit/s	Margin [%]	Margin [bit/s]	Total with margin [bit/s]
Background (50 keV – 300 keV)	72	4608.0	30	1382.4	5990.4
Background (3 keV – 2 MeV)	692	44288.0	30	13286.4	57574.4

Photon-by-photon “background” (50-300 keV) continuous acquisition & storage

VERY BRIGHT BURST PHOTON-BY-PHOTON (3 keV – 2 MeV)					
Component	evts	bit	Margin [%]	Margin [bit]	Total with margin [bit]
Very bright burst (100 counts/cm²/s + full band background, 50 s duration)	823650	52713600.0	30	15814080	68527680
Pre burst (full band background, 100 s duration)	76400	4889600.0	30	1466880	6356480
Post burst (full band background, 50 s duration)	38200	2444800.0	30	733440	3178240
				TOTAL	78062400

Triggered full band photon-by-photon acquisition and storage

COMMON BURST PHOTON-BY-PHOTON (3 keV – 2 MeV)					
Component	evts	bit	Margin [%]	Margin [bit]	Total with margin [bit]
Common burst (10 counts/cm²/s + full band background, 50 s duration)	116745	7471680.0	30	2241504	9713184
Pre burst (full band background, 100 s duration)	76400	4889600.0	30	1466880	6356480
Post burst (full band background, 50 s duration)	38200	2444800.0	30	733440	3178240
				TOTAL	19247904

SCIENTIFIC TELEMETRY

PDHU SRs				
	Sampling [s]	Packet size [byte]	Packet size [bit]	Rate [bit/s]
PDHU SR (4 quadrants, 3 energy bands, 7 timescales)	60	840	6720	112

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				TOTAL	19247904

TOTALS PER DAY (MARGINS INCLUDED)	
Component	bits/day
SR Telemetry budget	9676800
Photon list header	75340800
Background (50-300 keV)	517570560
Very bright burst photon-by-photo data (1 per day)	78062400
Common burst photon-by-photon (2 per day)	38495808
TOTAL [bits/day]	719146368
TOTAL [Gbits/day]	0.719

MASS & POWER BUDGETS

Mass

Item	Q.ty	Volume [cm3]	Material	Specific weight [g/cm3]	Unit Mass CBE [g]	Total Mass CBE [g]	DMM [%]	DMM [g]	Total Mass CBE + DMM [g]
P/L Total						1497.6		92.2	1587.8
Detector assembly	1					1178.34		64.32	1242.65
Detector PCB	1	19.9	FR4	1.95	38.81	38.81	5	1.94	40.75
ERM8-060 connector	2	0.82		3.00	2.46	4.92	5	0.25	5.17
Crystal Box	1	22.5	Stainless Steel	8.00	180.00	185.60	5	9.28	194.88
Crystal Lid	1	22.9	Stainless Steel	8.00	183.20	184.80	5	9.24	194.04
Tungsten Shield 0,20mm	1	1.6	Tungsten	19.10	30.56	30.33	5	1.52	31.85
Tungsten lat.Shield 0,20mm	2	0.44	Tungsten	19.10	8.40	16.30	5	0.82	17.12
Bottom Support Structure	1	8.4	Stainless Steel	8.00	67.20	66.70	5	3.34	70.04
Top Support Structure	1	11.9	Stainless Steel	8.00	95.20	92.80	5	4.64	97.44
Filter	1	0.4	Kapton+Ni frame	8.90	1.00	1.00	30	0.30	1.30
Screws ISO 4762 - M2,5x8	4	0.07	Steel	7.80	0.55	2.18	20	0.44	2.62
Screws ISO 4762 - M3x12	9	0.15	Steel	7.80	1.17	10.53	20	2.11	12.64
Screws ISO 7045 - M2x5	16	0.03	Steel	7.80	0.23	3.74	20	0.75	4.49
Dowel pin 2x12	2	0.038	Steel	7.80	0.30	0.59	20	0.12	0.71
SDD tile	12	0.21	Silicon	2.33	0.49	5.87	30	1.76	7.63
SDD glue	12				0.22	2.64	30	0.79	3.43
Frame	12	0.132	ABS	1.06	0.14	1.68	5	0.08	1.76
Frame K	12	0.09	Kovar	8.30	0.75	8.96	5	0.45	9.41
Wrapping	60		DF2000MA		0.18	10.80	5	0.54	11.34
Optical coupling	60	0.26	Silicone	1.03	0.27	16.07	5	0.80	16.87
Crystal	60	1.26	Ce:GAGG	6.51	8.20	492.16	5	24.61	516.76
Elastomer springs	60	0.02	Laird Tflex 300	1.78	0.03	1.85	30	0.56	2.41
PDHU	1					97.87		4.89	102.76
ISIS iOBC	1				114.00	97.87	5	4.89	102.76
BEE/TIME	1					89.47		4.47	93.94
CSAC	1				35.00	35.00	5	1.75	36.75
ERF8-060 connector	2	1.55		3	4.65				
BEE	1	15.9	FR4	1.95	31.01	54.47	5	2.72	57.19
PSU	1					72.28		7.49	77.69
EMI shield	1					9.38	5	2.55	9.85
PICO DC-DC	1				12.00	12.00	20	2.40	14.40
PCB	1	17.7	FR4	1.95	34.52	50.90	5	2.55	53.45
Other items						59.67		11.03	70.71
Internal harness	1					30.00	30	9.00	39.00
PCB long Spacers	12	0.3	Aluminium 6082	2.71	0.81	10.08	5	0.50	10.58
PCB short Spacers	4	0.08	Aluminium 6082	2.71	0.22	0.72	5	0.04	0.76
Guide-rail	4	0.5	Stainless Steel	8.00	4.00	15.20	5	0.76	15.96
Ribs screws ISO 7046 - M2x6	4	0.03	Steel	7.80	0.23	0.94	20	0.19	1.12
MLI thermal blanket	1		Sheldahal 146454		1.00	1.00	20	0.20	1.20
Thermal shield vs BUS	1	0.89	Teflon	1.95	1.74	1.74	20	0.35	2.08

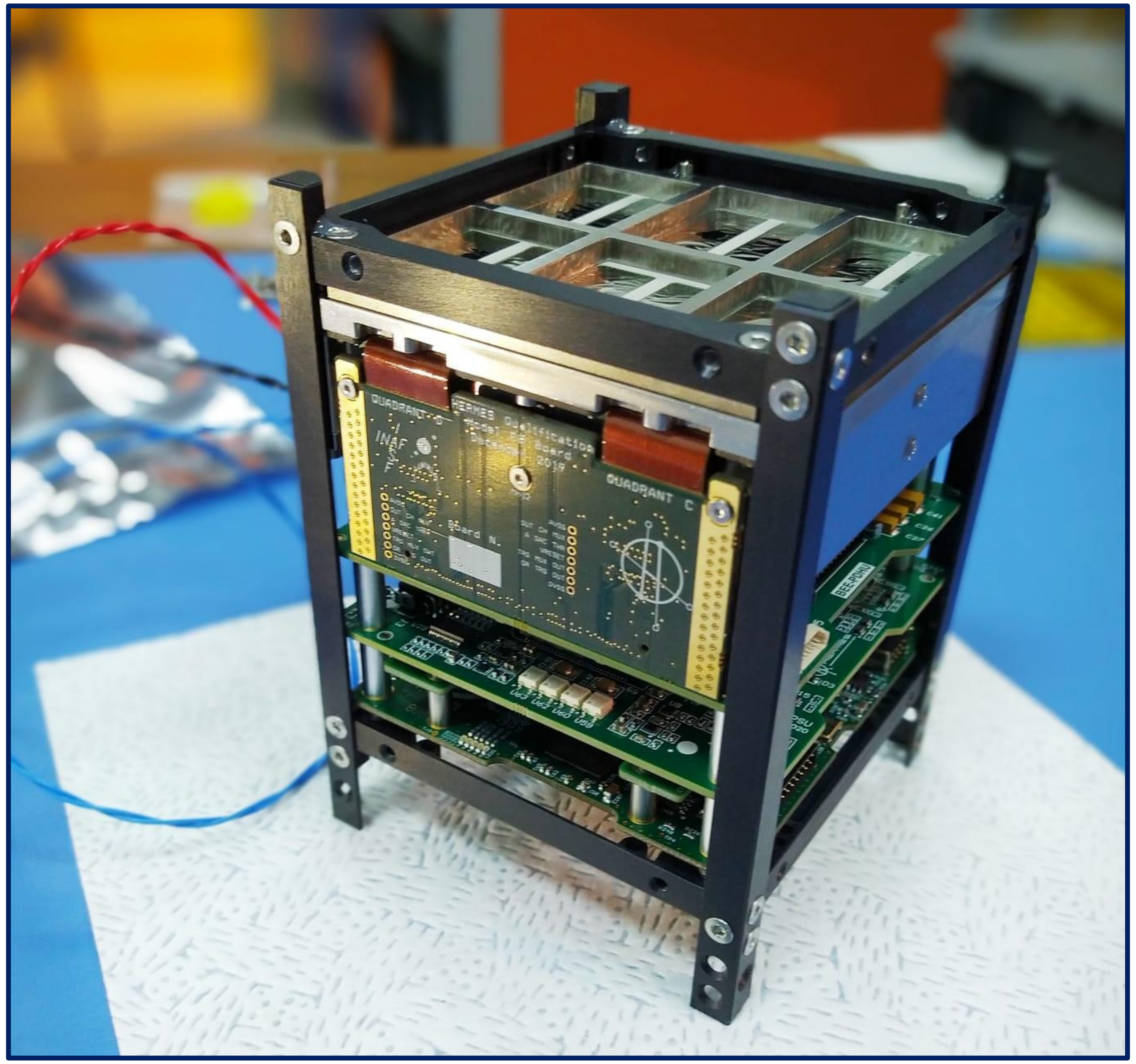
Power

Item	No	Power [mW]	Total [mW]	Contingency [%]	Contingency [mW]	Total with contingency [mW]	Conv. factor	Total with margin & conv. factor [mW]
P/L with system margin				**30**				**6227.8**
P/L	**1**		**3112.3**		**706.8**	**3819.1**		**4790.6**
Detector assemby	**1**		**175.3**		**52.6**	**227.9**		**327.7**
SDD	120	0.8	96.5	30	28.9	125.4	0.8	156.8
LYRA-FE	120	0.3	32.4	30	9.7	42.1	0.6	70.2
LYRA-BE	128	0.4	46.5	30	13.9	60.4	0.6	100.7
PDHU	**1**		**550.0**		**27.5**	**577.5**		**577.5**
ISIS iOBC	1	550.0	550.0	5	27.5	577.5	1	577.5
BEE	**1**		**1615.0**		**529.5**	**2144.5**		**2929.6**
FPGA	1	1000.0	1000.0	40	400.0	1400.0	0.8	1750.0
ADC	4	50.0	200.0	20	40.0	240.0	0.6	400.0
CSAC	1	140.0	140.0	5	7.0	147.0	0.8	183.8
Other components	1	275.0	275.0	30	82.5	357.5	0.6	595.8
PSU	**1**		**772.0**		**97.2**	**869.2**		**955.9**
HV DC-DC converter	1	672.0	672.0	10	67.2	739.2	1	739.2
Control electronics	1	100	100.0	30	30.0	130.0	0.6	216.7

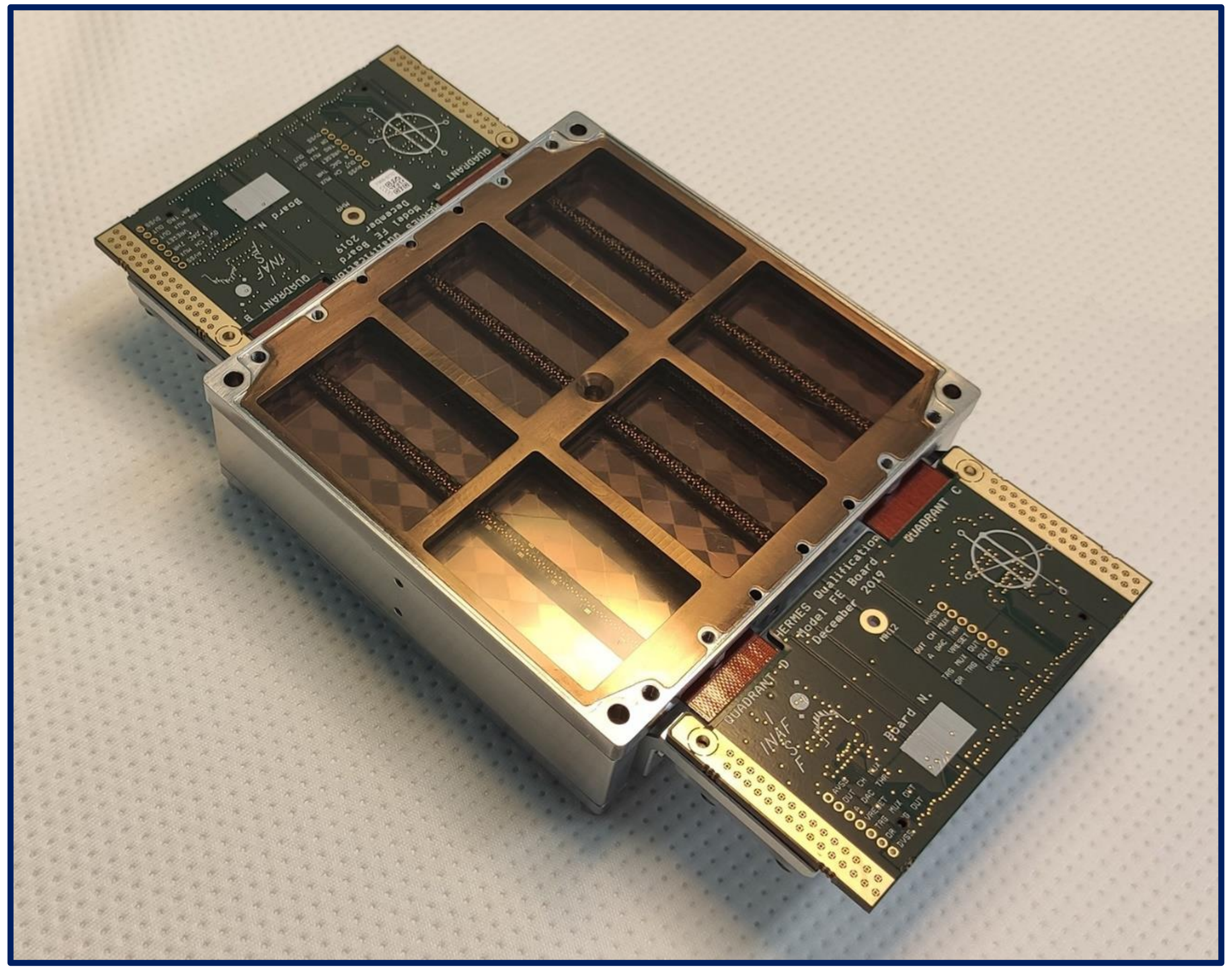
P/L DEMONSTRATION MODEL

P/L DM integrated in July-August 2020 with:

- Mechanical assembly
- Optical filter
- FEE board equipped with:
- 4 LYRA-BE ASICs (one per DA quadrant)
- 120 LYRA-FE ASICs (30 per quadrant)
- 3 in-spec SDD arrays (30 channels of Quadrant A)
- 1 in-spec SDD array, correspondent to 10 channels of Quadrant D
- 8 dummy SDD arrays, mechanically representative
- 60 GAGG crystals
- Fully representative optical coupling and crystal preload pads
- Tungsten shields



DM PERFORMANCE

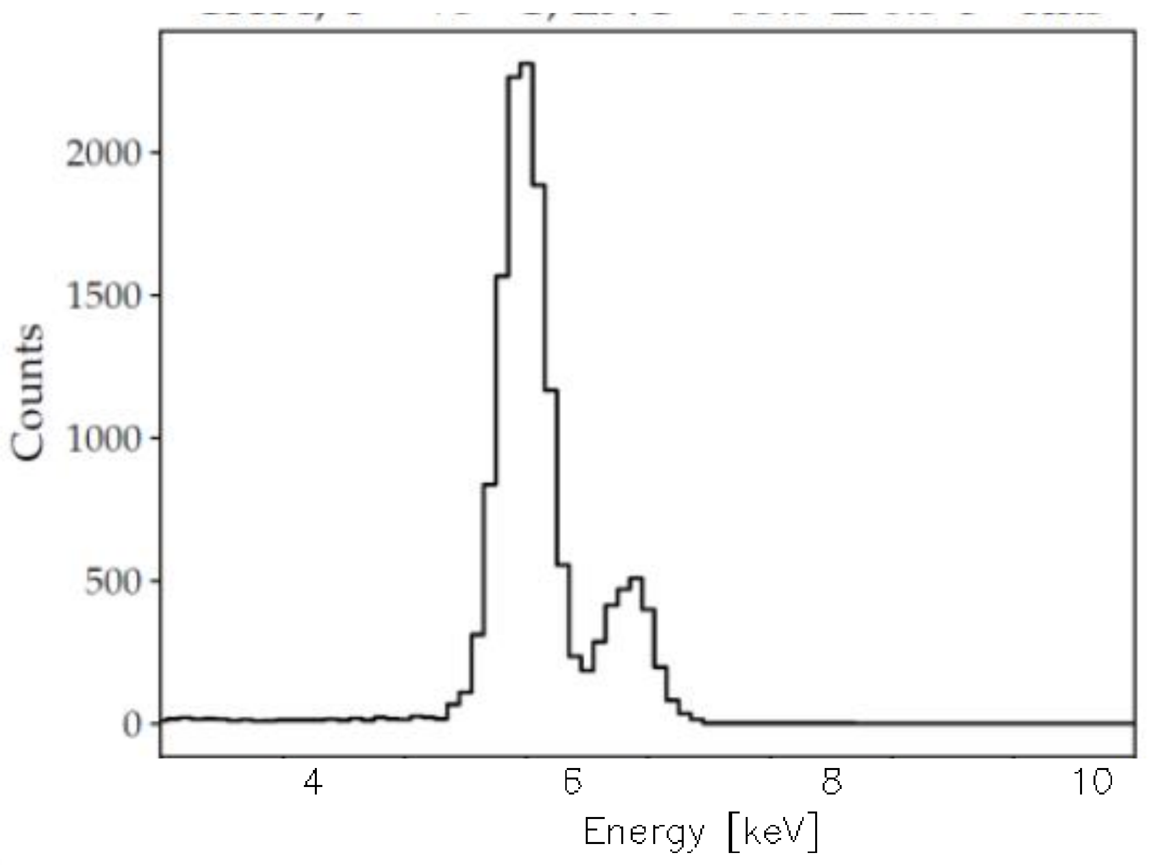


Sensor ID	Anode number	Anode current @ 20 °C [pA]
W010-4	1	44
	2	40
	3	35
	4	83
	5	33
	6	62
	7	76
	8	30
	9	34
	10	37
W115-3	1	33
	2	90
	3	46
	4	44
	5	33
	6	34
	7	85
	8	44
	9	42
	10	35

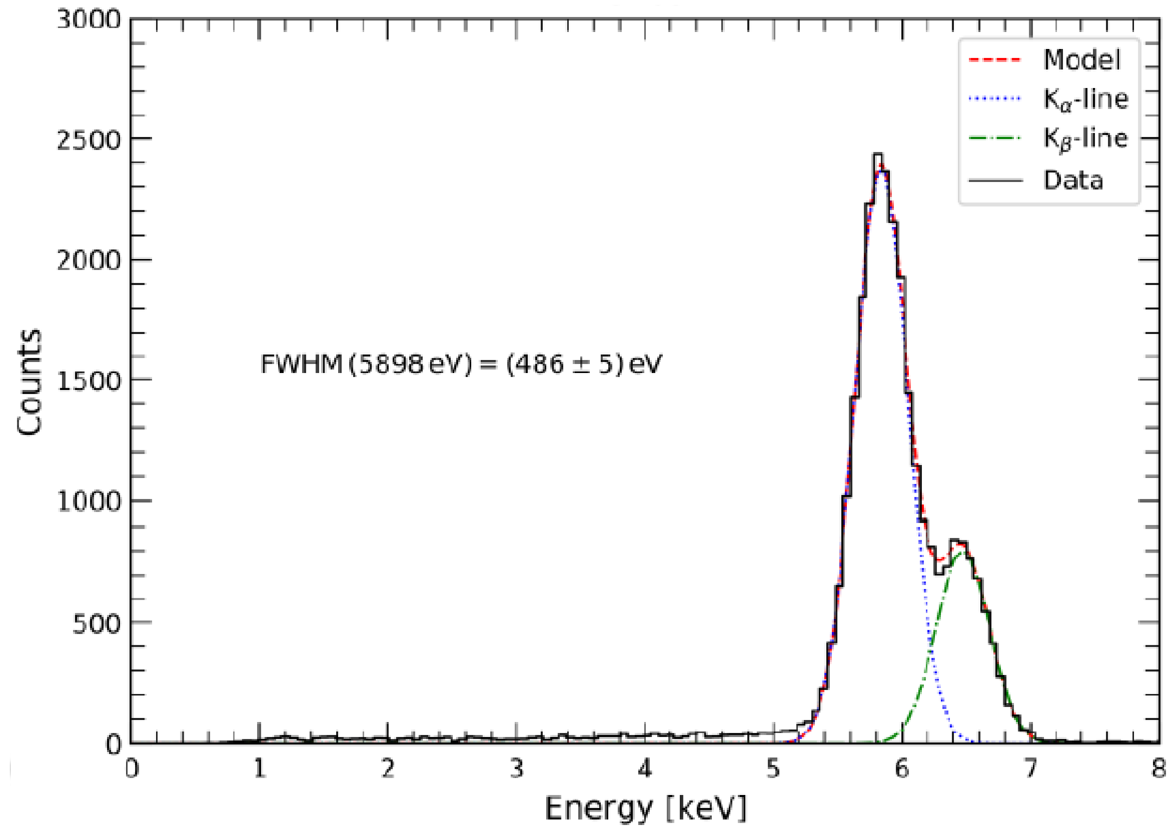
Sensor ID	Anode number	Anode current @ 20 °C [pA]
W140-3	1	41
	2	77
	3	88
	4	63
	5	60
	6	42
	7	86
	8	83
	9	61
	10	60
W248-3	1	26
	2	53
	3	51
	4	49
	5	48
	6	23
	7	47
	8	58
	9	47
	10	43

High performance SDD arrays representative of FM detectors

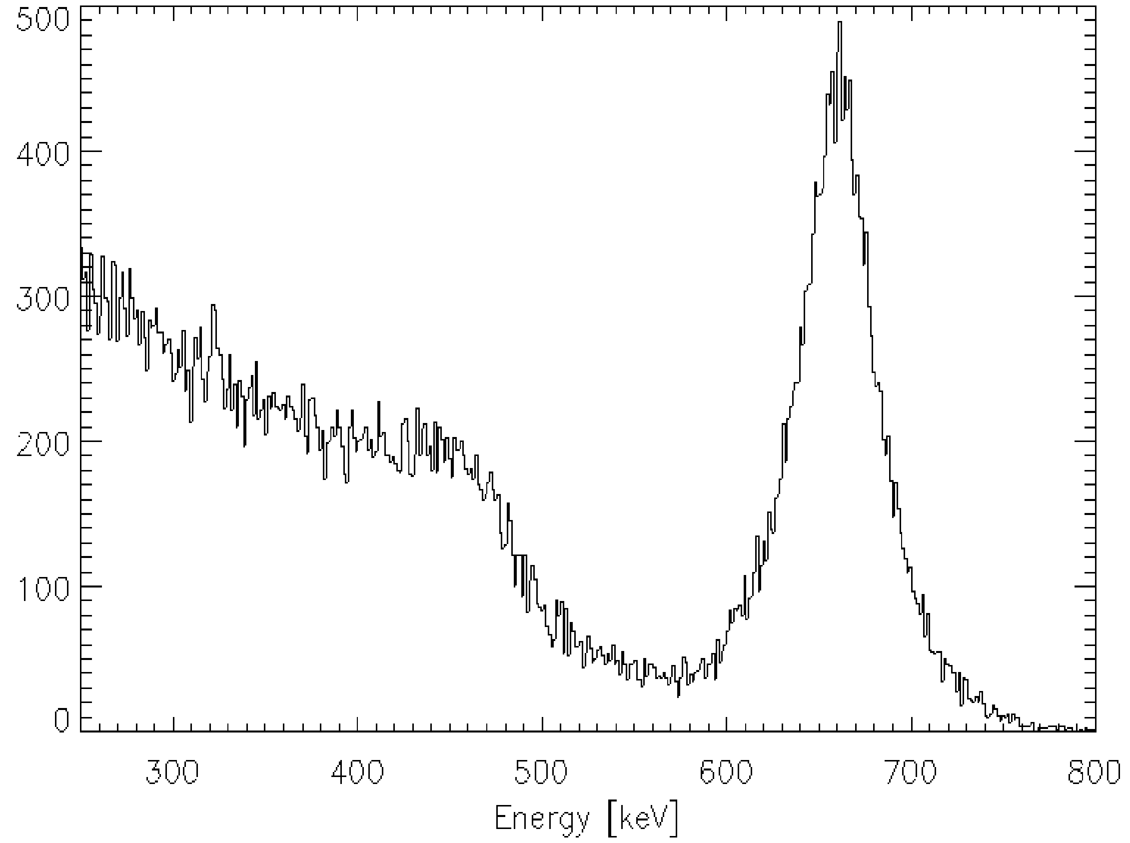
X-mode BOL



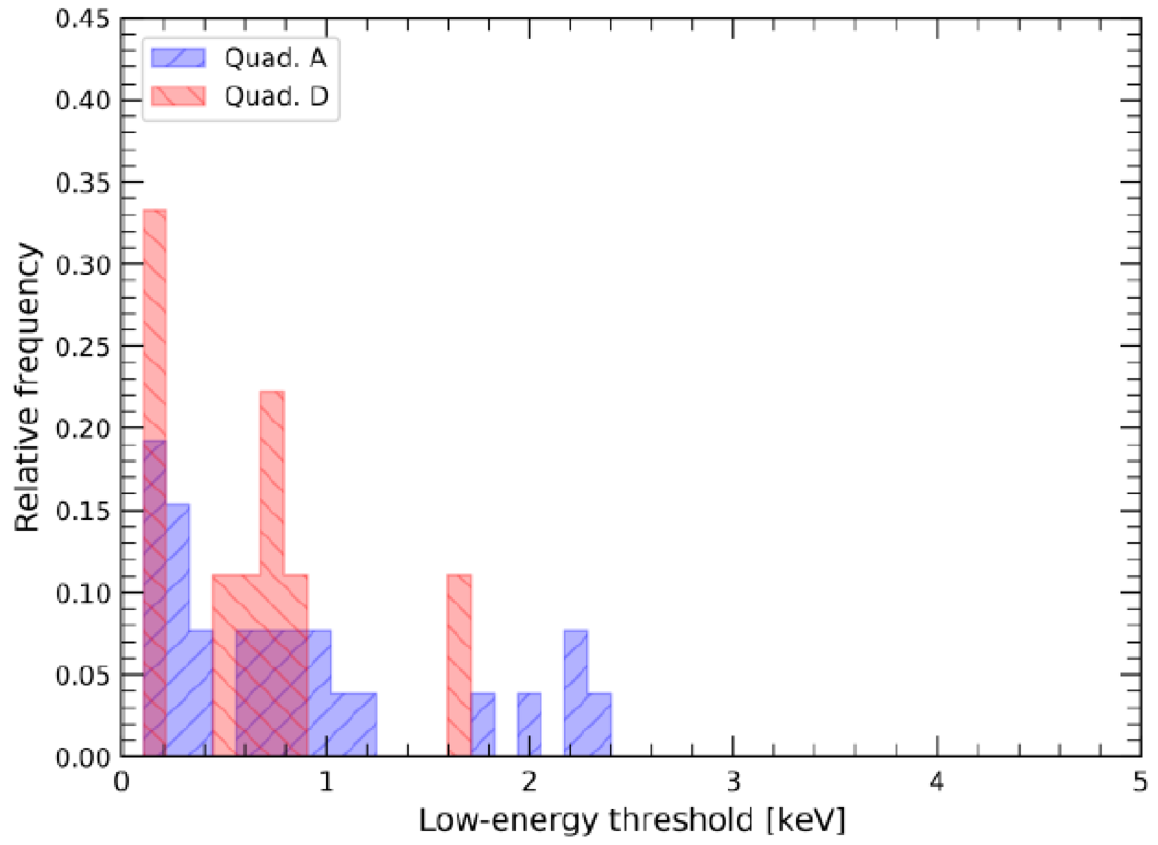
X-mode EOL



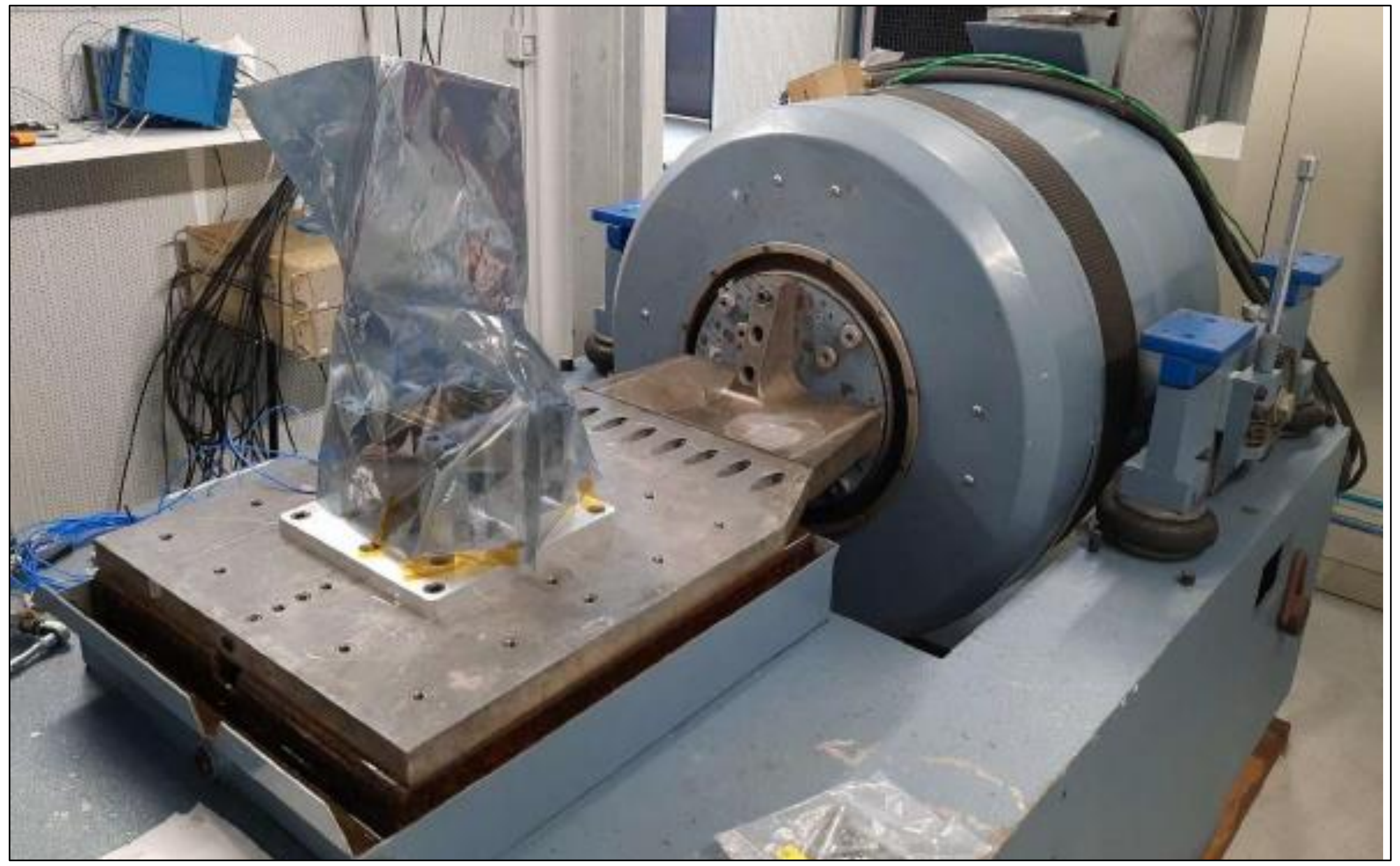
S-mode EOL

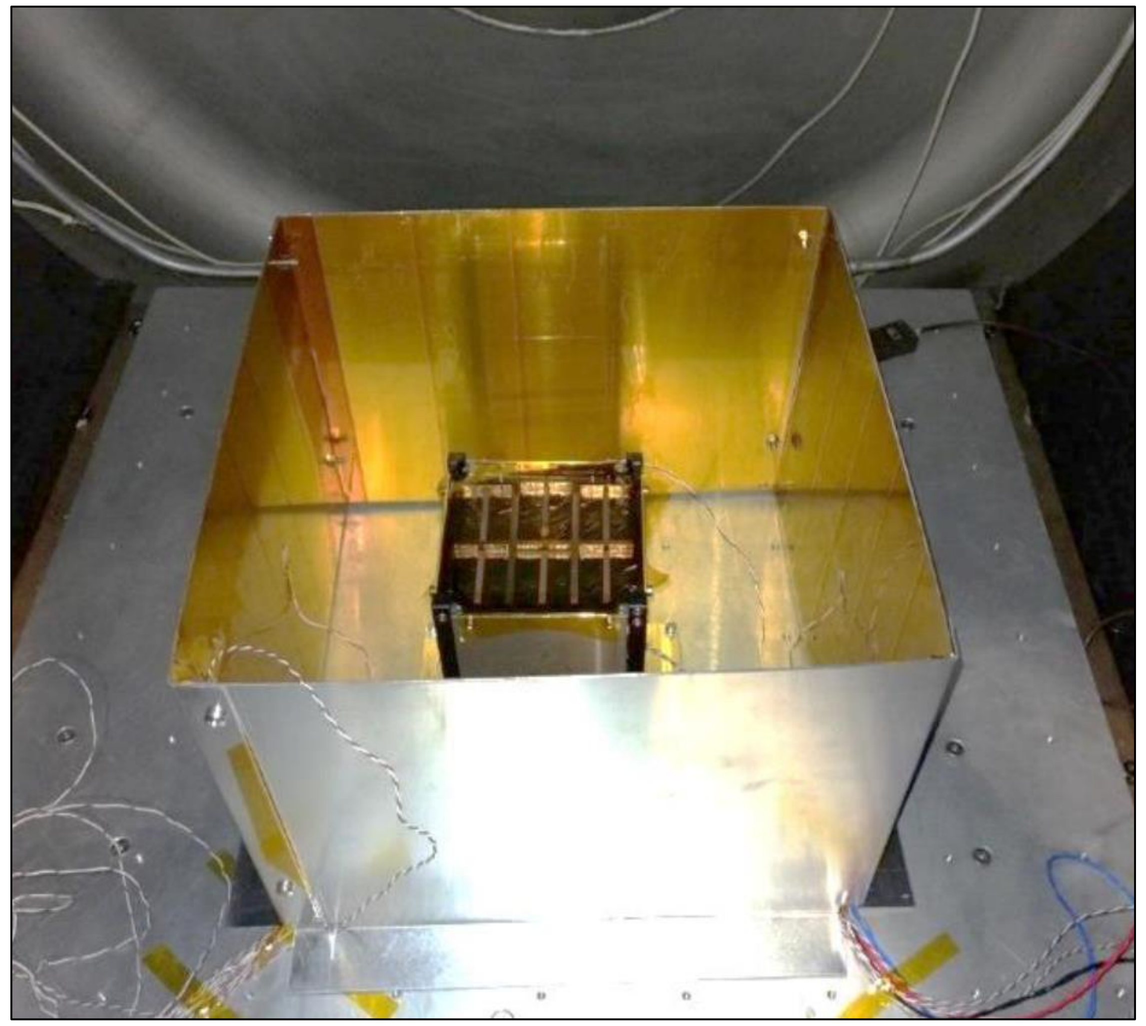


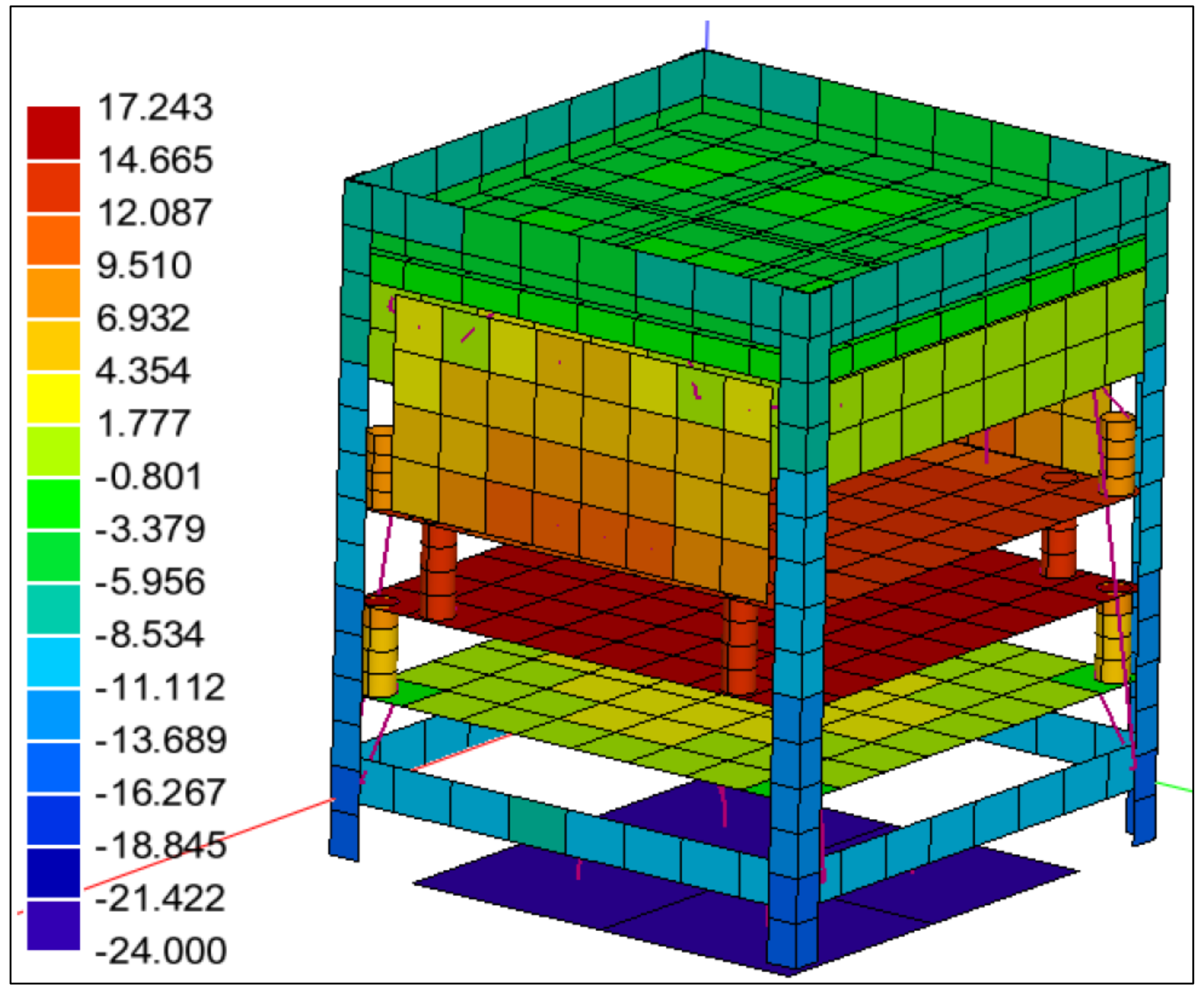
Lower E threshold EOL

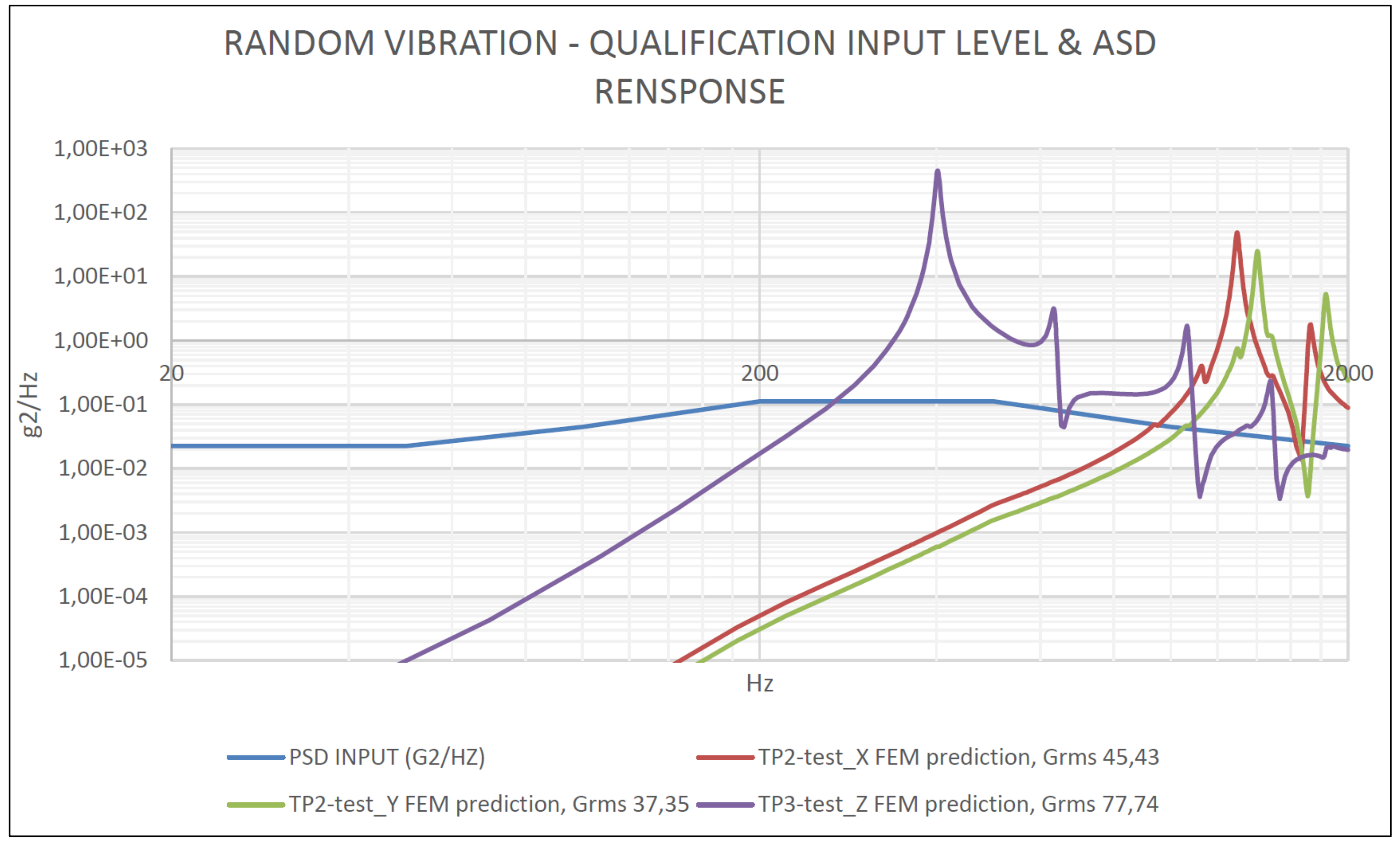


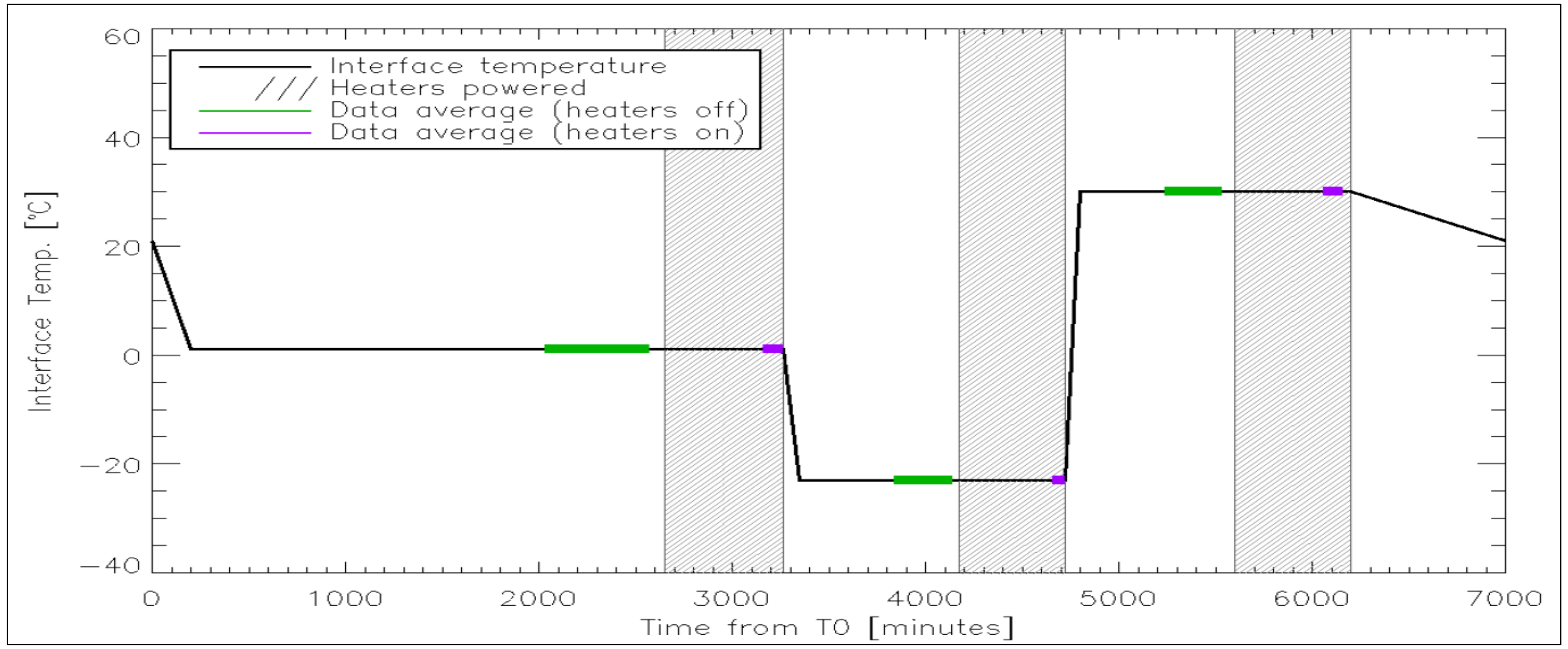
DM ENVIRONMENTAL TESTS









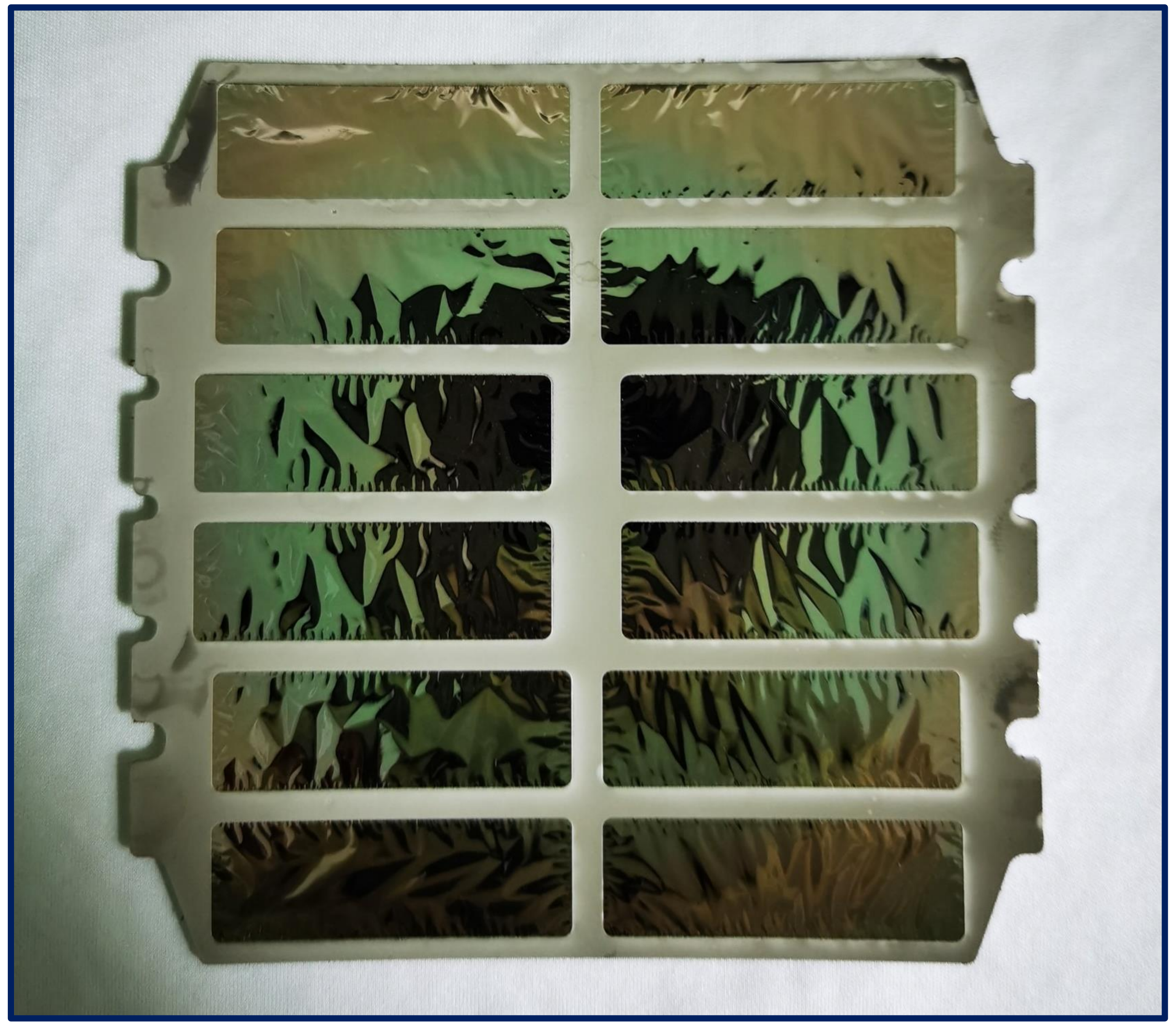


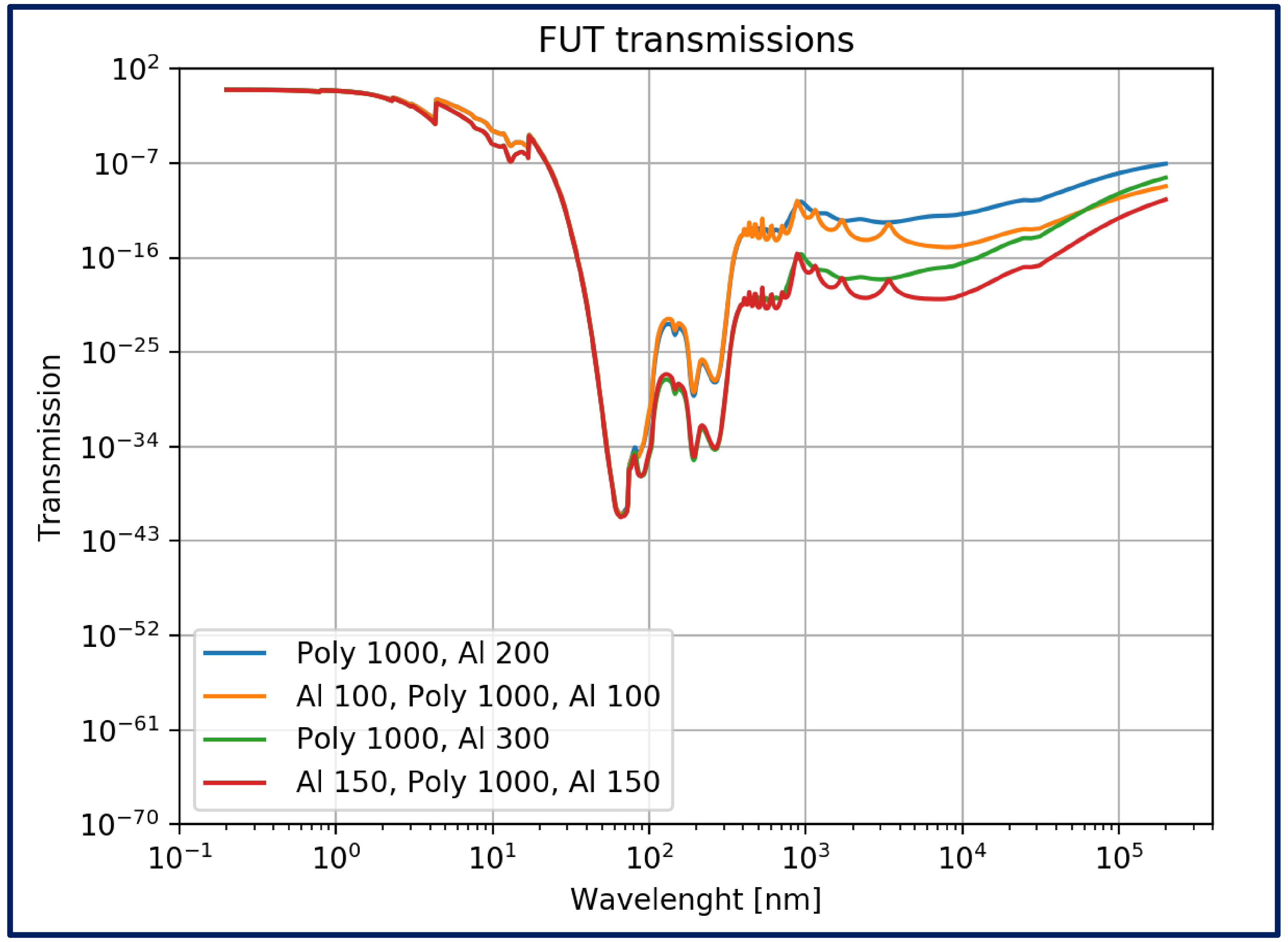
P/L Mechanical design verified with Ariane V qualification levels (+3db) @ PoliMi shaker facility

P/L Thermal design verified with thermal balance test (TBT) @ PoliMi TVAC facility


THANK YOU

OPTICAL FILTER





Filter is part of optical and thermal design of the P/L → prime task is to prevent NIR/O/UV light from reaching the SDD (leakage current generation) for wavelengths shorter of 1130 nm (Silicon band-gap).

Required transmission is $< 10^{-7}$ in 10^2-10^5 nm

HERMES filters manufactured by IHEP (Beijing).

THERMAL ENVIRONMENT AND RADIATION DAMAGE